Gamma/pi0 Detector of the Nose Cone Calorimeter

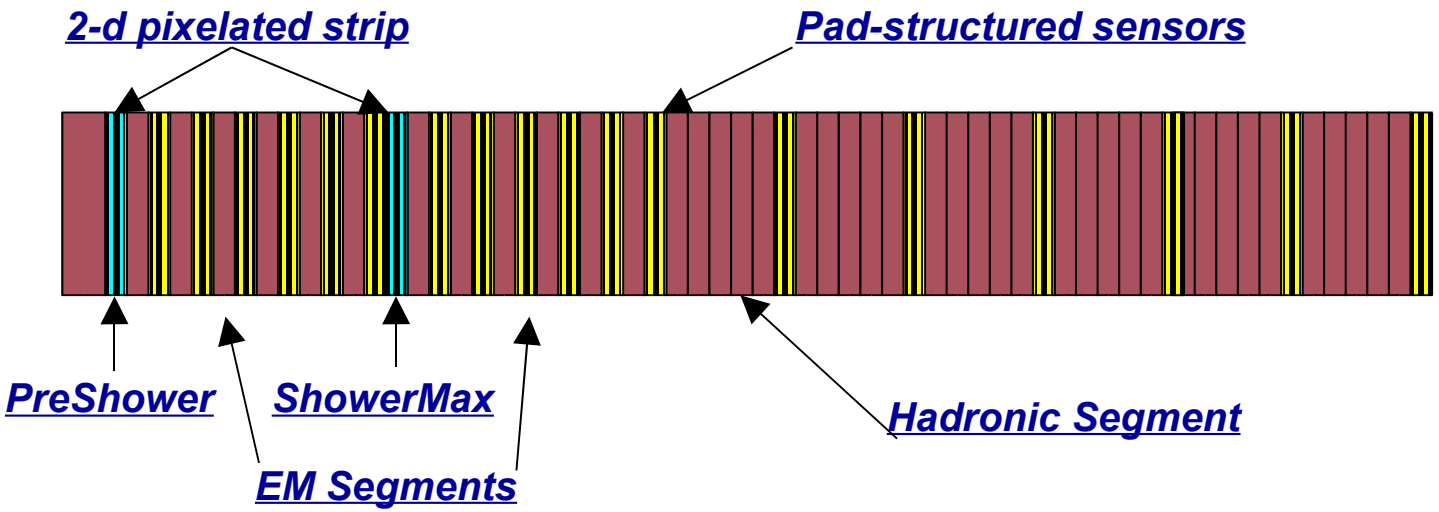
1) Design concepts

- Electromagnetic module
- Stripixel readout using SVX4
- Readout module
- FEM module

2) Status of prototyping

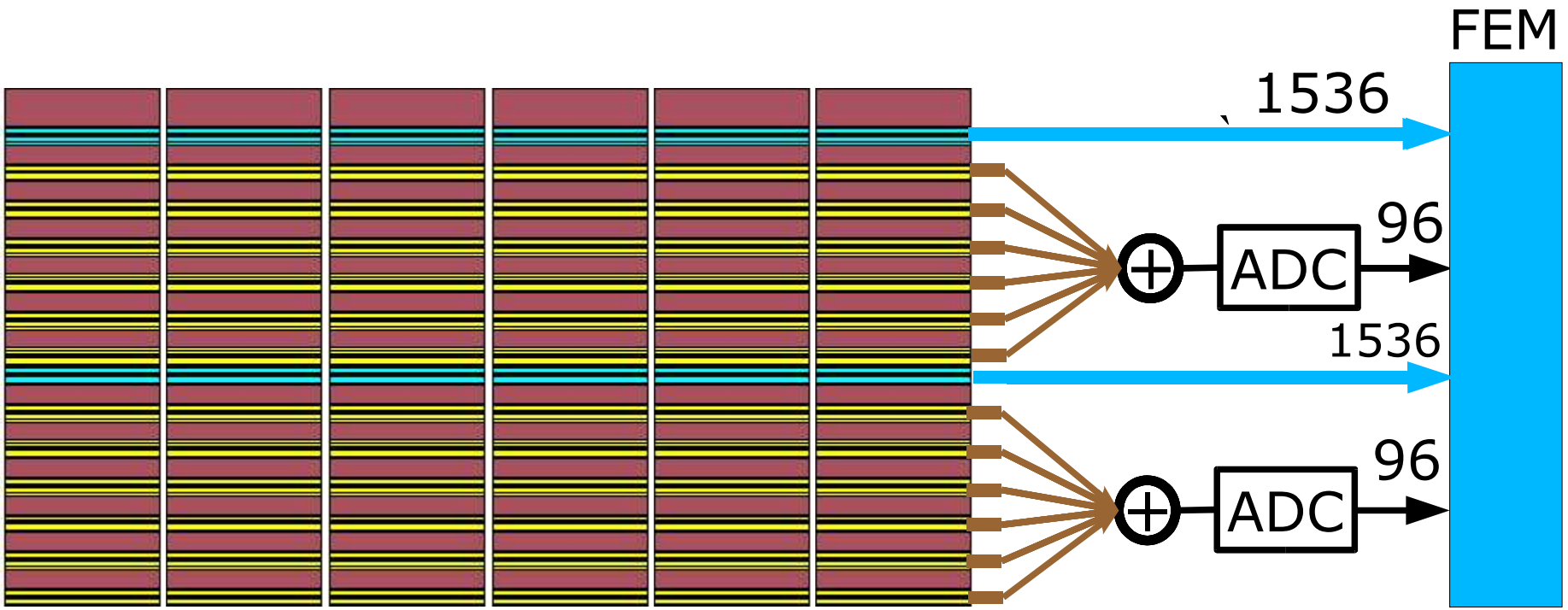
- Stripixel detector
- Front-end electronics

Longitudinal structure of a single calorimeter tower



EM segment:
Very efficient photon-pi0 identifier discriminating between individual electromagnetic showers and overlapping photons from high momenta pi0.

EM Brick



Goal: One FEM per brick.

Parameters of the NCC Stripixel Detectors

Sensor height [mm]	64
Sensor width [mm]	64
Strip length [mm]	64
Strip pitch [mm]	0.5
Strip thickness [mm]	0.6
Bulk strip capacitance [pf]	2.5
Interstrip capacitance [pf]	?
Strip orientation	XY
Bias voltage [V]	+ 150-175
Breakdown voltage [V]	300
Expected occupancy	~ 1%

Strips per sensor	256
Number of sensors	336
Number of SVX4 chips	672
Total number of channels	86016

SVX4 parameters

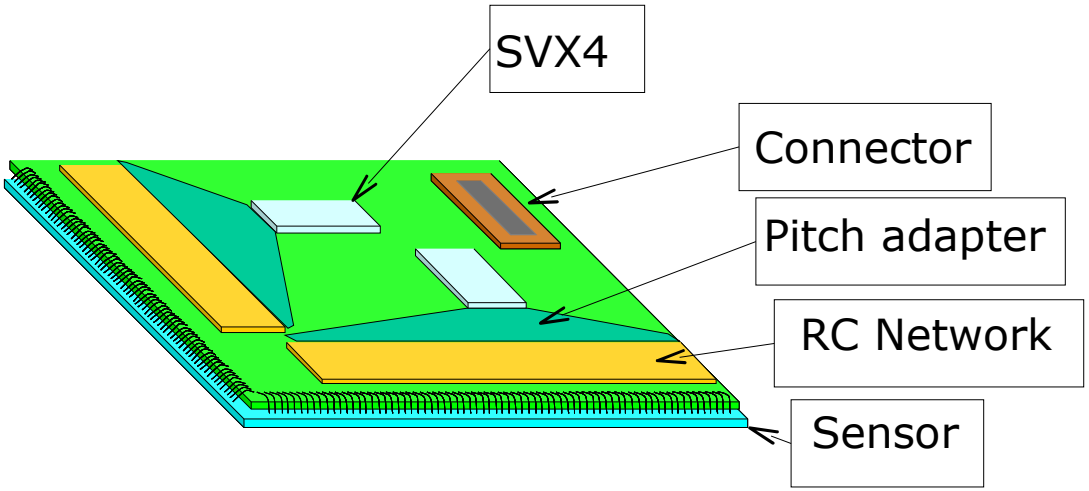
Number of channels: 128
ADC: 8 bit
Input bonding pad pitch: 48μm

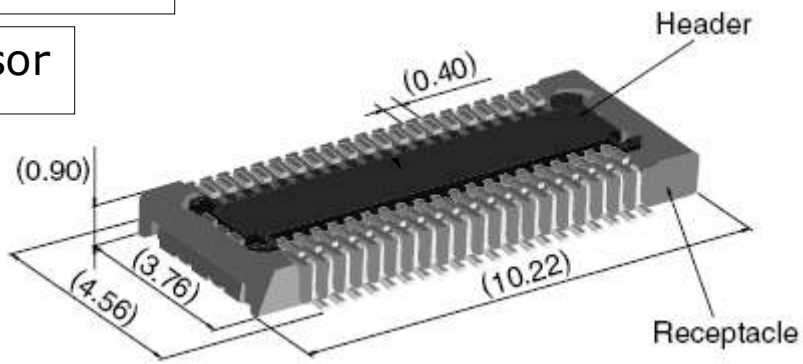
B. Preamp:
1. Input pulse polarity: **Positive**
2. Gain (feedback capacitor): 3mV/fC
3. External load capacitance: 10pF to 50pF
5. Risetime 0-90%: adjustable in a range that includes 60-100ns for any allowed load
6. Risetime adjustment: 4 bits minimum
7. Noise (ENC): 2000e or less for a 40pF load using double correlated sampling with 100ns integration t.
8. DC open loop gain: >2500 (>95% charge collection from 40pF)
9. Linearity: Linear response for pulses up to 20fC non-linearity < 0.25mV at output
10. Dynamic range: **>200fC**

C. Pipeline
1. Dynamic range **40 fC, (10 MIP)**

Readout Module (ROM)

Space limitation: The thickness of the assembled board should be less than 5 mm



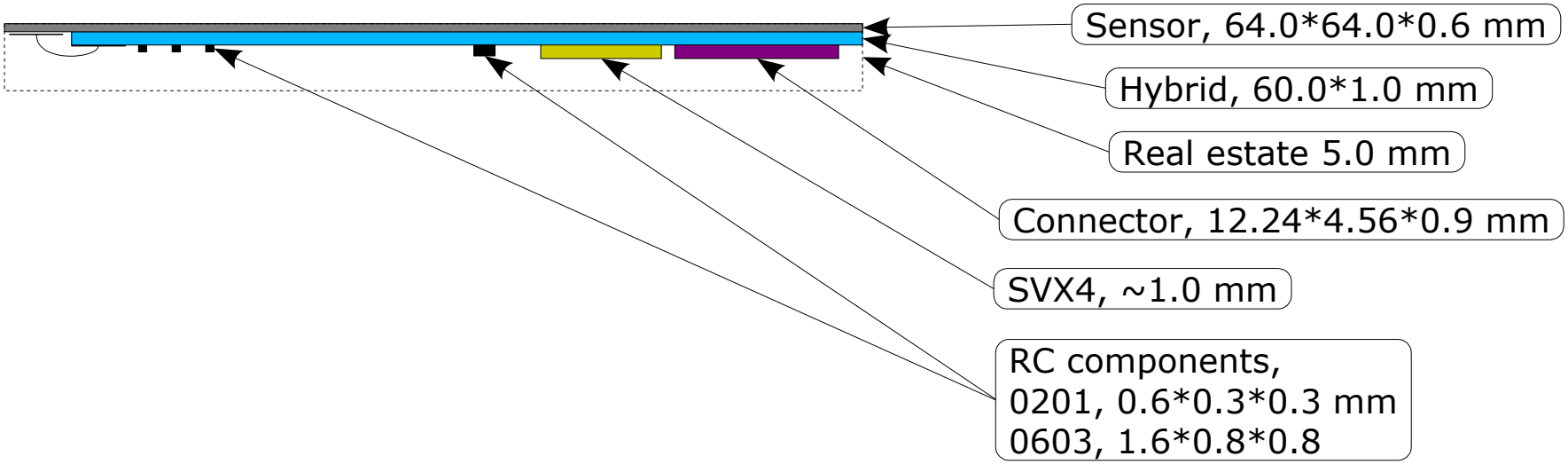


Connector: Hirose DF30, 50 pin
Pitch adapter: Al on silicon
RC Network: SMT 0201 components

Environment monitoring using **1-Wire interface**:

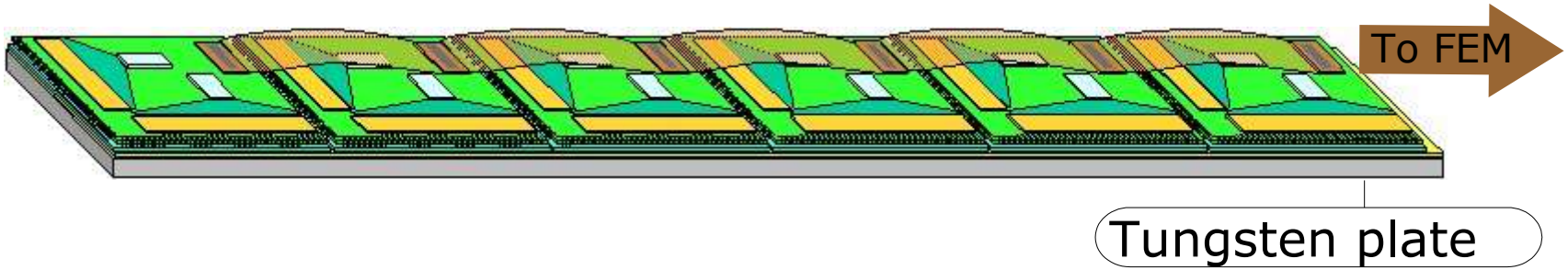
- Temperature
- Leakage current

Readout Module Cross Section

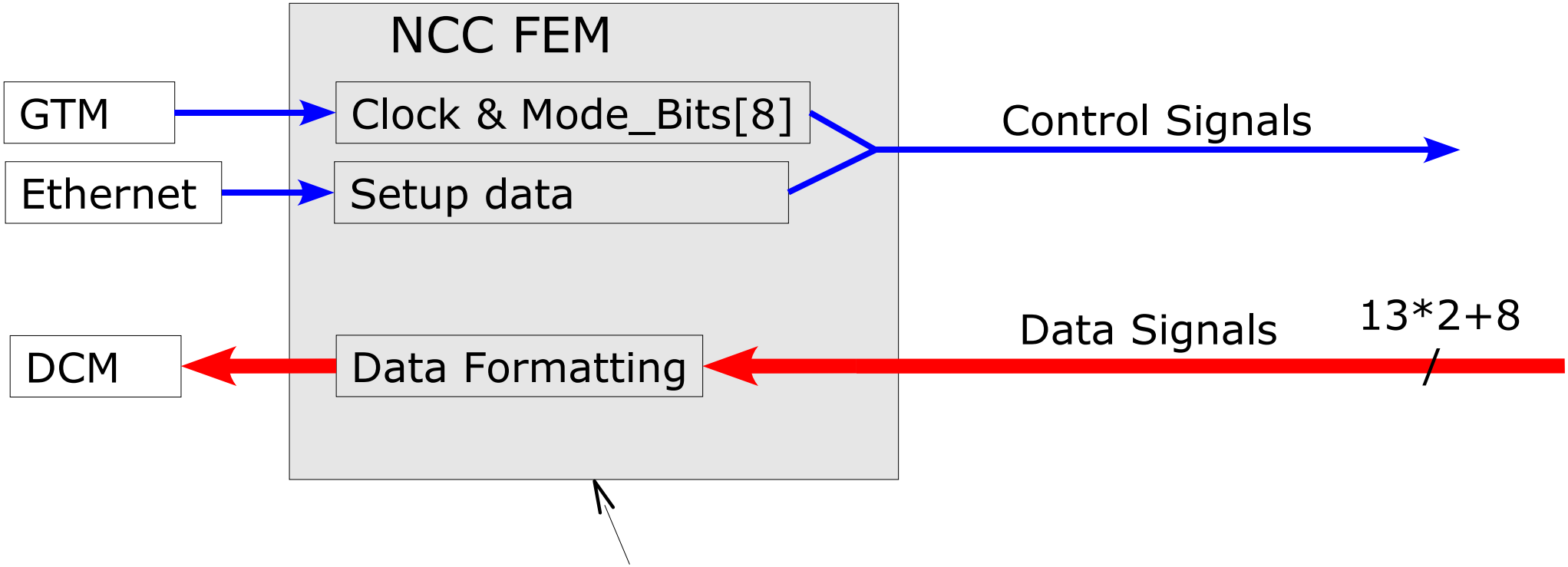


Readout Ladder

Six or seven sensors with the readout hybrids are glued to a carrier board.
All SVX4 chips are dasy chained and connected to a FEM module.
The FEM is 64mm*100mm*10mm board located on the carrier board.
The low voltage power and the bias voltage for sensor supplied by a pilot board mounted on the magnet.
Only one bias voltage supply per ladder can be routed due to a limited number of wires.



Readout Diagram



Under development
CPU: MFC5271, Ethernet, JTAG
OS: OpenTCP
Data traffic: XILINX Spartan3

Readout Conditions

These are the conditions that must be satisfied:

1) The system must be capable of handling multiple Level-1 triggers occurring while waiting for the first event to be digitized and sent into the FEM. The current requirement is to buffer 5 events, but the SVX4 is only capable of storing 4, so the one event should be buffered inside the FEM.

2) The digitization must be complete in 40 usec.

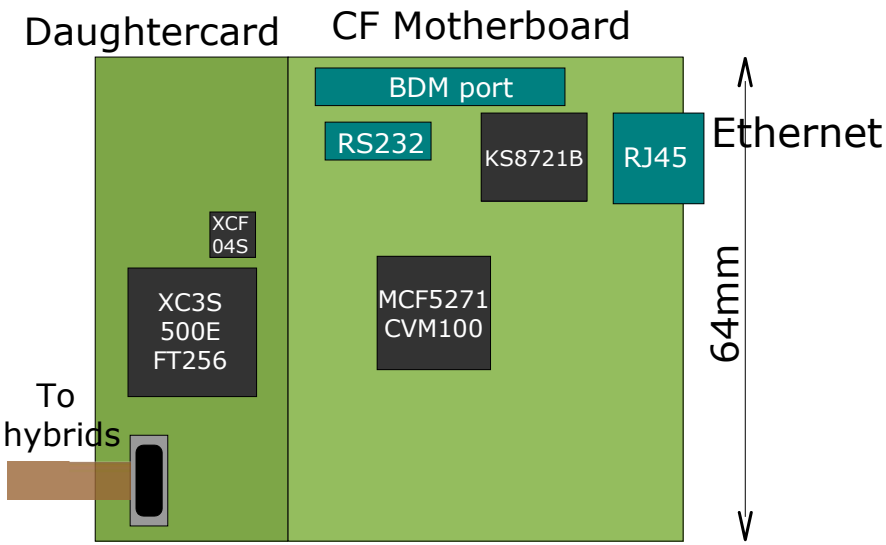
3) The data must be transferred to the FEM in another 40 usec.

4) The system must be capable of digitizing one event at the same time that it is transferring the first event so that as soon as one event is transferred we can start transferring the next event.

Readout Time

Back-end clock [Mhz]	53
Digitization time [us]	**2.42**
Readout time (no pedestal suppression)	
Number of hits	128
Number of clocks	129
Readout time of the single SVX4 [us]	2.43
Number of SVX4 in the chain	14
Data size [kB]	3.53
Readout time of the chain [us]	**34.08**

NCC-FEM (Front-End Module)



NCC-FEM board

Currently we are prototyping using software compatible M5235BCC evaluation board

Hardware:

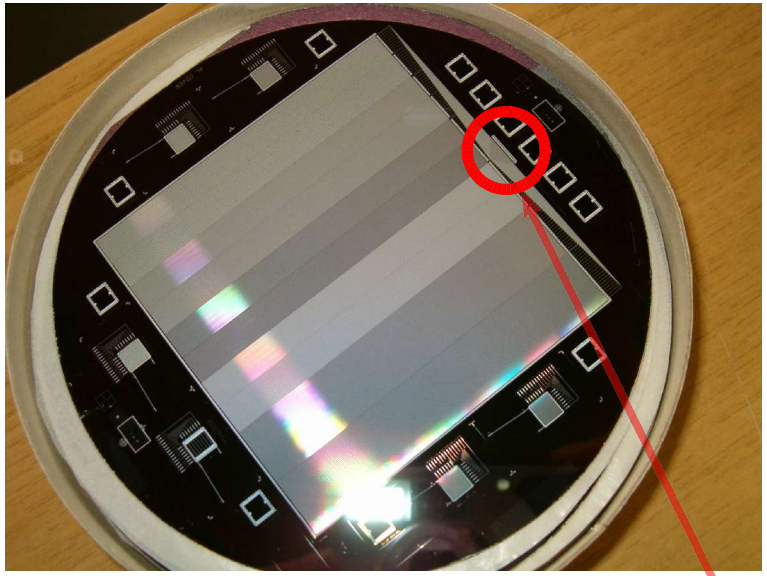
MCF5271 – ColdFire 100 Mhz CPU
64 KB SRAM, 8KB Cache, Ethernet, RS232, I2C, GPIO, JTAG. Cost: $10.

XC3S & XCF – XILINIX Spartan3 FPGA, three models will fit: 250E, 500E or 1200E. Cost $22 + $8

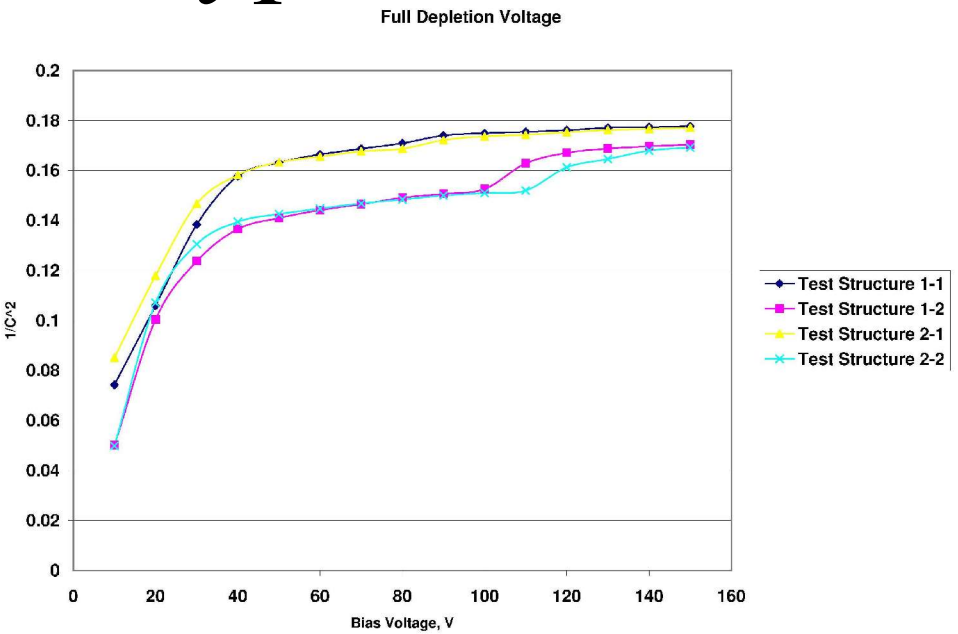
KS8721B, RJ45 - Ethernet for slow control, FPGA programming, downloading,

RS232 and BDM – for debugging

Status of the Prototype Sensor



Si wafers designed in BNL ID and produced by ELMA in Russia



Test Diode structure shows satisfactory IV curves

Failure:

All stripixel test structures on all wafers have very low breakdown voltage (30 V). Shorts or Shottky structures.

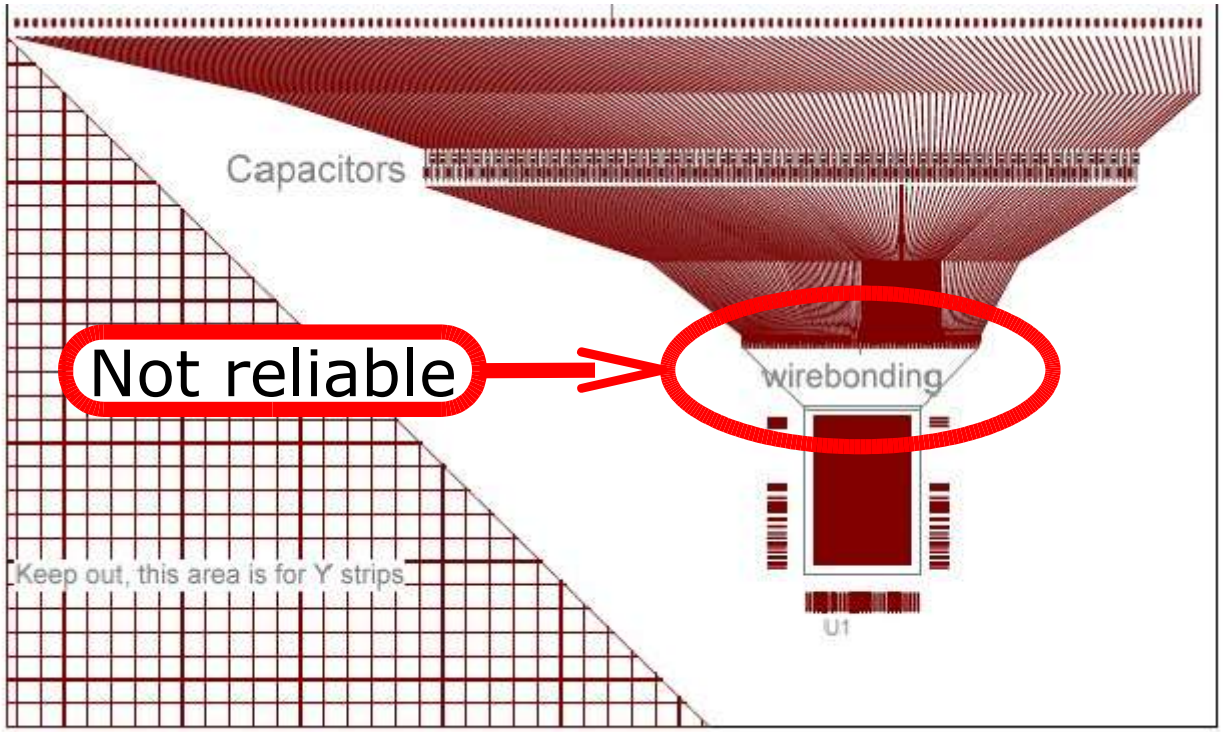
Plan:

Try to save the stage. Cut off the pads, remove SiO2 from traces, if lucky then characterize the sensor.

<u>Need new design, preferable made by the factory.</u>

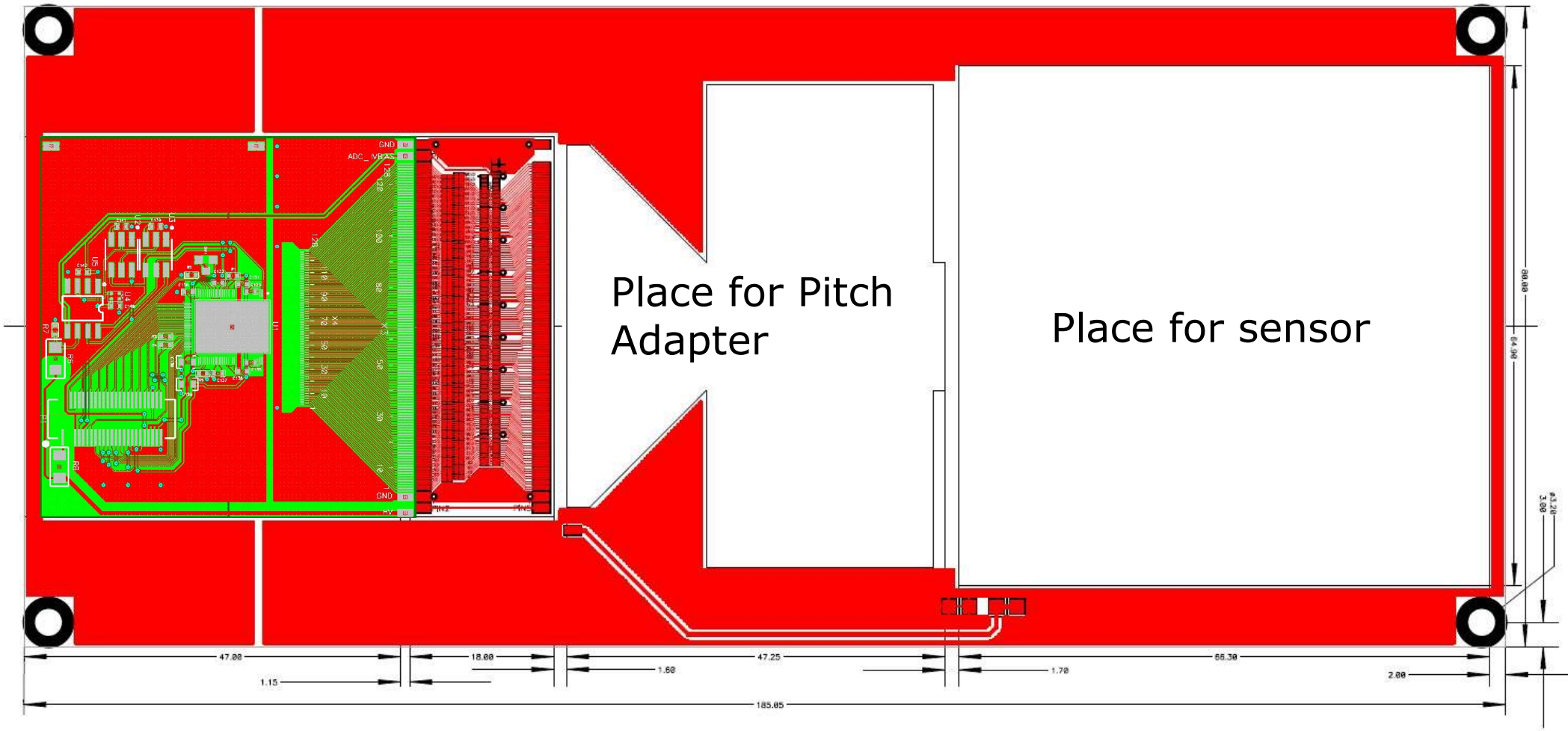
PCB Design for Dyconex

DYCOstrate technology – ultra high wiring density
min. lines/ min spaces = 25/35 μm
min. via diameter (blind via/PTH) = 50/70 μm



Conclusion: Too expensive

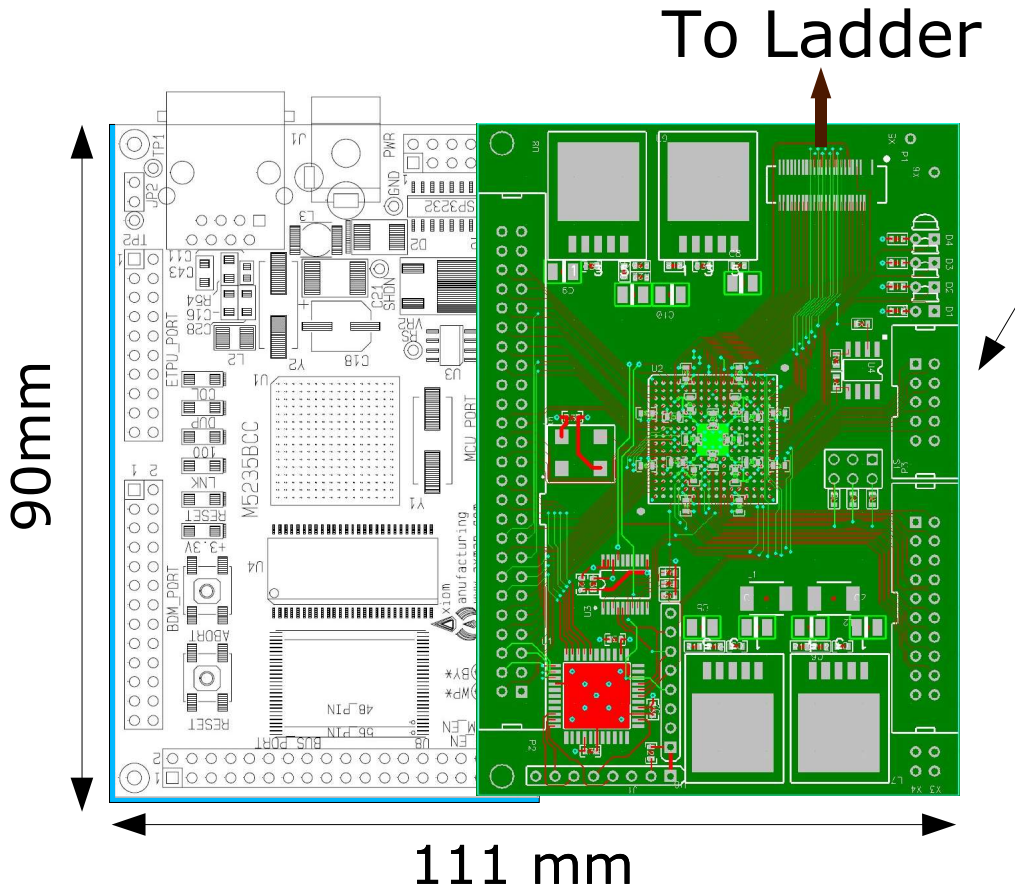
Prototype PCB with Pitch Adapter



Designed by Sergey Basilev group, Dubna.
Wire spacing: 75 μm.

Status: Being manufactured at ID BNL.

PCB of the prototype FEM



CFFPGA board, designed with help from Sergey Basilev group, Dubna

Software status:

Development using a eval. board M5235BCC:

Tested and accepted:

Quadros+OpenTCP

Tested: uclinux (nfs, ftp, ssh)

Solution found for Remote FPGA downloading.

Status: Ready for manufacturing at ID BNL.