Feasibility of the ALICE Pixel Detector Readout Chip for PHENIX

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- **Origin of the device: CERN/RD19/ALICE**
- **Specifications $\Leftrightarrow$ PHENIX requirements**
- **a couple of interesting material related issues**

CERN RD19 Collaboration:

Development of Hybrid and Monolithic Silicon Micropattern Detectors

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- *Divisional affiliation:* EP
- *Notes:* Beam : - ; Approved : 910627, 920206, 930211, 940210, 950209 ; Status : In Progress

chip generation		pixel size [μm^2]	bump ⌀ [μm]	pixels per chip	technology [μm]	electronics specification
1)	LAA (1988)	200 × 200	30	9 × 12	SACMOS 3	current + voltage amplifier, discriminator, 1 bit memory
2)	OMEGA-D (1991)	75 × 500	30	64 × 16	SACMOS 3	charge amplifier, discriminator, leakage current compensation, shift register output, tunable delay
	OMEGA2 (1993)	75 × 500	30	64 × 16	SACMOS 3	+ improved uniformity
3)	LHC1 (1995)	50 × 500	10	128 × 16	SACMOS 1	+ adjustable delays, facilities to test/mask individual pixels; fine-tune delays/thresholds
4)	LHC2 (1997)	30 × 590	10	128 × 2 test chip	MIETEC 0.5	+ radiation tolerance
5a)	ALICE1 (1999–)	50 × 400 (425)	20	256 × 32 near-final chip	MIETEC 0.25	rad-tol. 30 Mrad; delay line + trigger logic fit ALICE specs; 10 (40) MHz clock
5b)	LHCb (1999–)	67 × 500	20	256 × 32 near-final chip	MIETEC 0.25	+ 40 MHz clock (clock lines wider)

Experiments:

- **WA 94**

adapted for

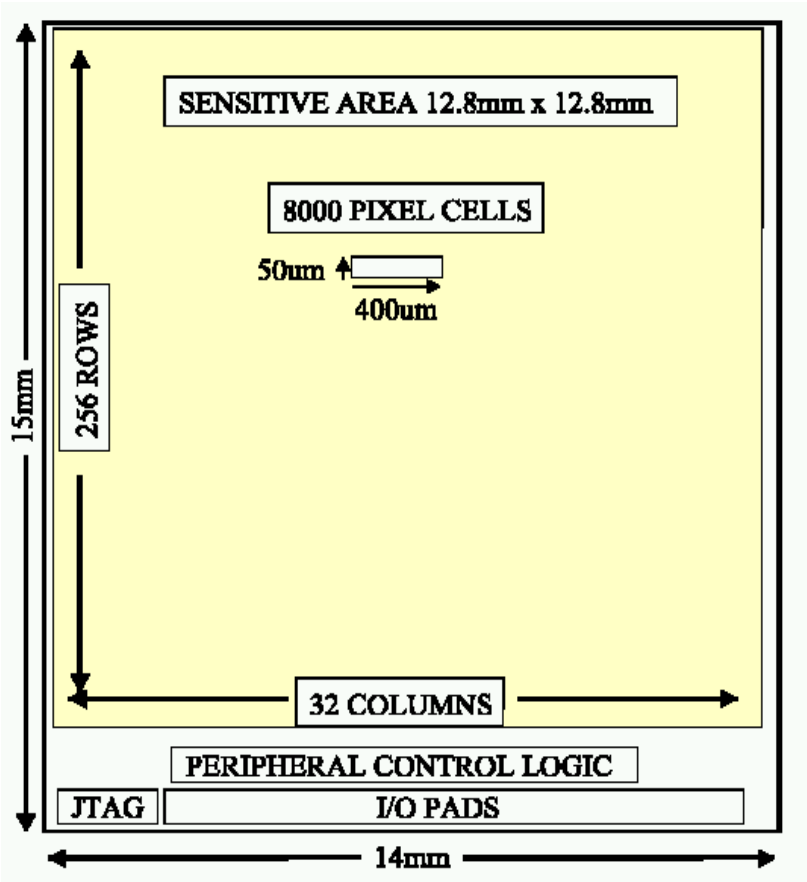
- **DELPHI/LEP2** [1)]
- **WA 97**
- **NA 57 (NA50)** [2)]
- **ALICE/NA60**
- **LHCb**

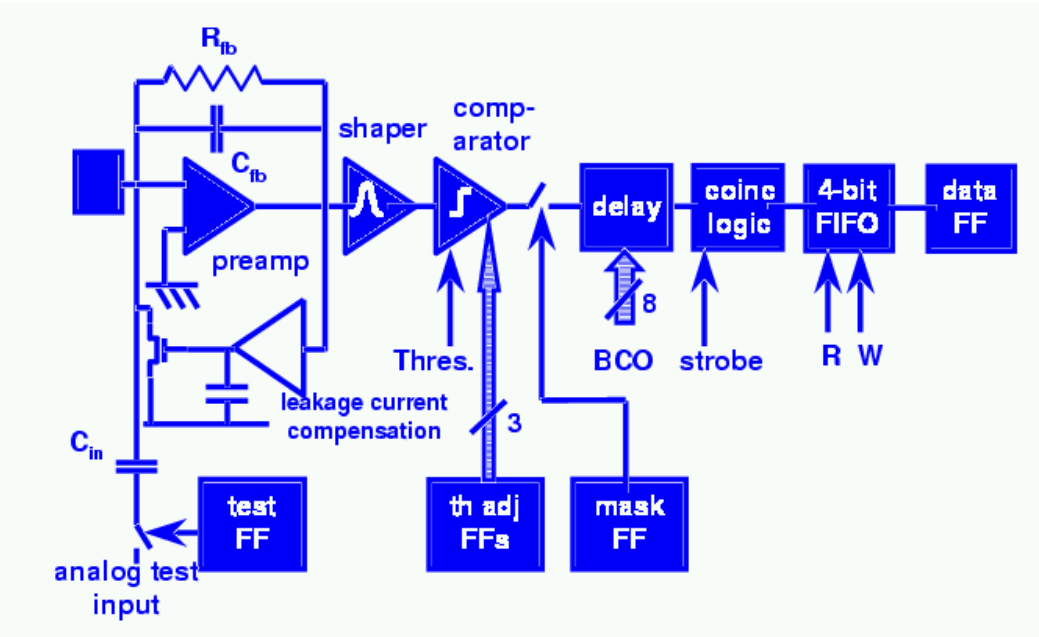
The only existing 'large scale' (>1M) pixel detectors to date::

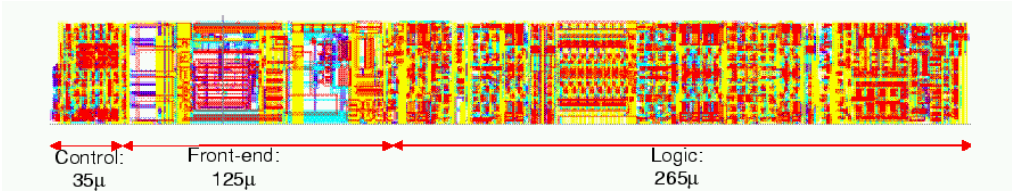
1) DELPHI Very Forward Tracker. First application of active pixel detectors in a collider exp., 1995–2000. Zero suppression integrated into frontend electronics (Sparse Data Scan).

2) First physics measurements with dominant active pixel detector contribution; fixed–target experiments.

ALICE Pixel Readout Chip



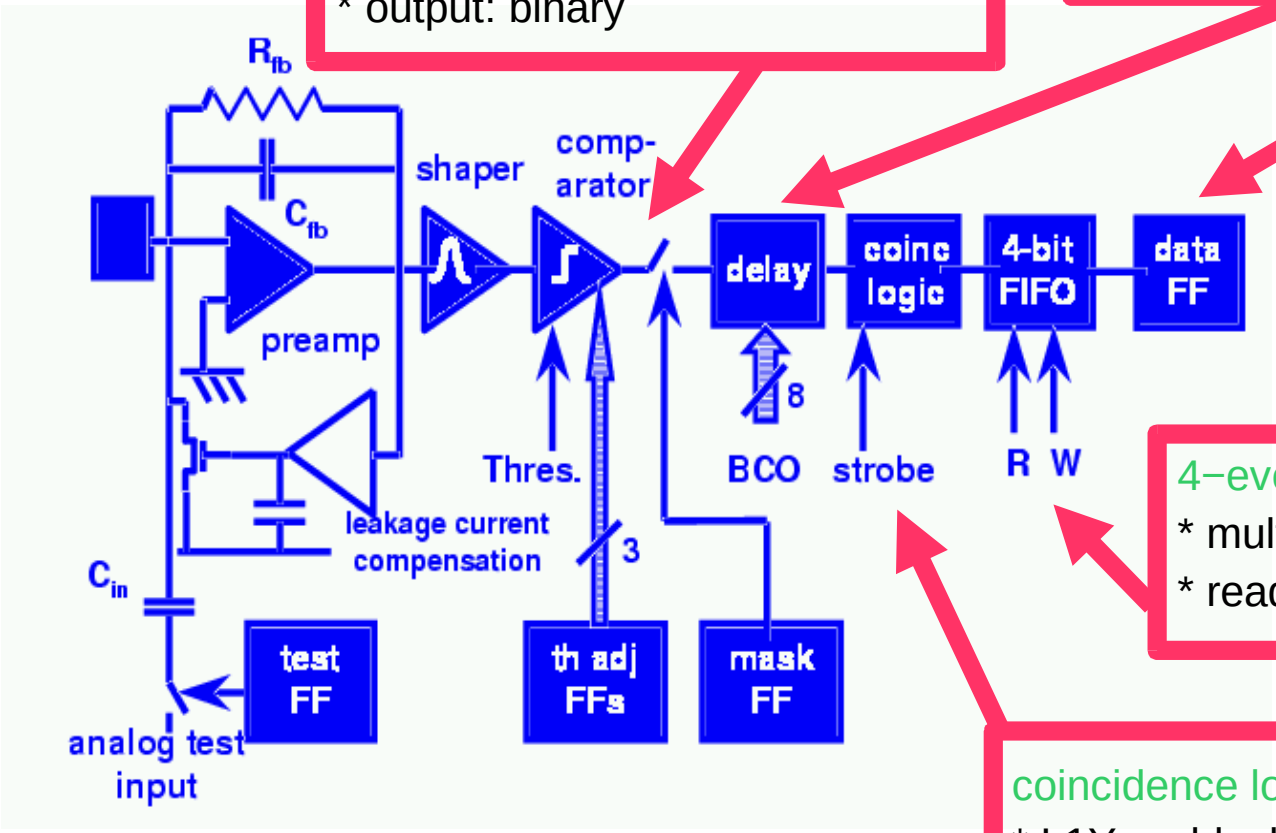




~2.2 cm^2, 0.7W analog
0.4W digital

comparator/discriminator:
* adjustable threshold > 1200 e^-
* global/chip + fine−tuning/pixel
* rms: 150 e^- (noise: 100−150 e^-)
* output: binary

delay:
* enable−logic
* stores for duration of trigger latency (adjustable, max. 5.5 µs)



readout:
* 32 bit shift register
* 256 clock ticks, 10 (40) Mhz
  ⇒ 25.6 (6.4) µs/chip

4−event FIFO:
* multi−event "de−randomising" buffer
* readout on L2Y

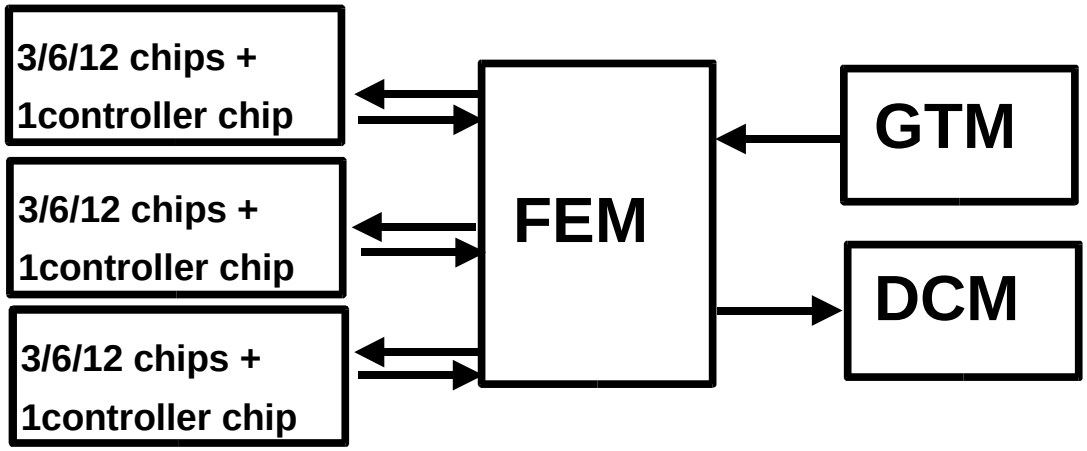
coincidence logic:
* L1Y: − block input to delay unit
  − write result into FIFO
  − reset delay unit
* L1N: go on with front−end

analog (preamp + 2 shapers):
continuous, fast: t < 200 (150) ns

refs: analog: R. Dinapoli et al., CERN−2000−010
digital: K. Wyllie et al., CERN−99−09

PHENIX DAQ/ trigger requirements

* RHIC beam clock 9.4 MHz 106 ns BCO
* L1 trigger: < 40 BCOs, i.e. 4.3 μs
* complete readout of PHENIX detector systems:
  - GL1 imposes a programmable minimum time for each readout cycle (currently 40 μs)
  - min. 40 μs, max. 80 μs
* subsystems have 5−event FIFOs per design (not stringent)
* zero−suppression is performed in DCM's.
  however: pixel hit information is very sparse. Job for controller chip (FPGA ?)



System issues regarding material

* option for thin wafers:
  - wafers down to ~50 μm 'thickness' are available in commercial products as 'smart cards'
  - thinning of standard wafers by grinding
  - example: DISCO (www.disco.co.jp)

* cooling aspects:
  - NA60: first application of cryogenic silicon technology in high energy physics experiment;
  - beam−scope (strips/BNL, electronics/CERN) in vacuum pipe up to 10^9 p or ions /s
  - cooling: steel pipe of ~0.8mm Ø, loop over detector module; T = 80 − 130 K (liquid nitrogen)
  - test beam to verify detector concept: operational after

$$10^{14} \text{ Pb ions/cm}^2 = 90 \pm 40 \text{ Grad}$$