

# **RIKEN/CERN pixel electronics/bus R&D plans**

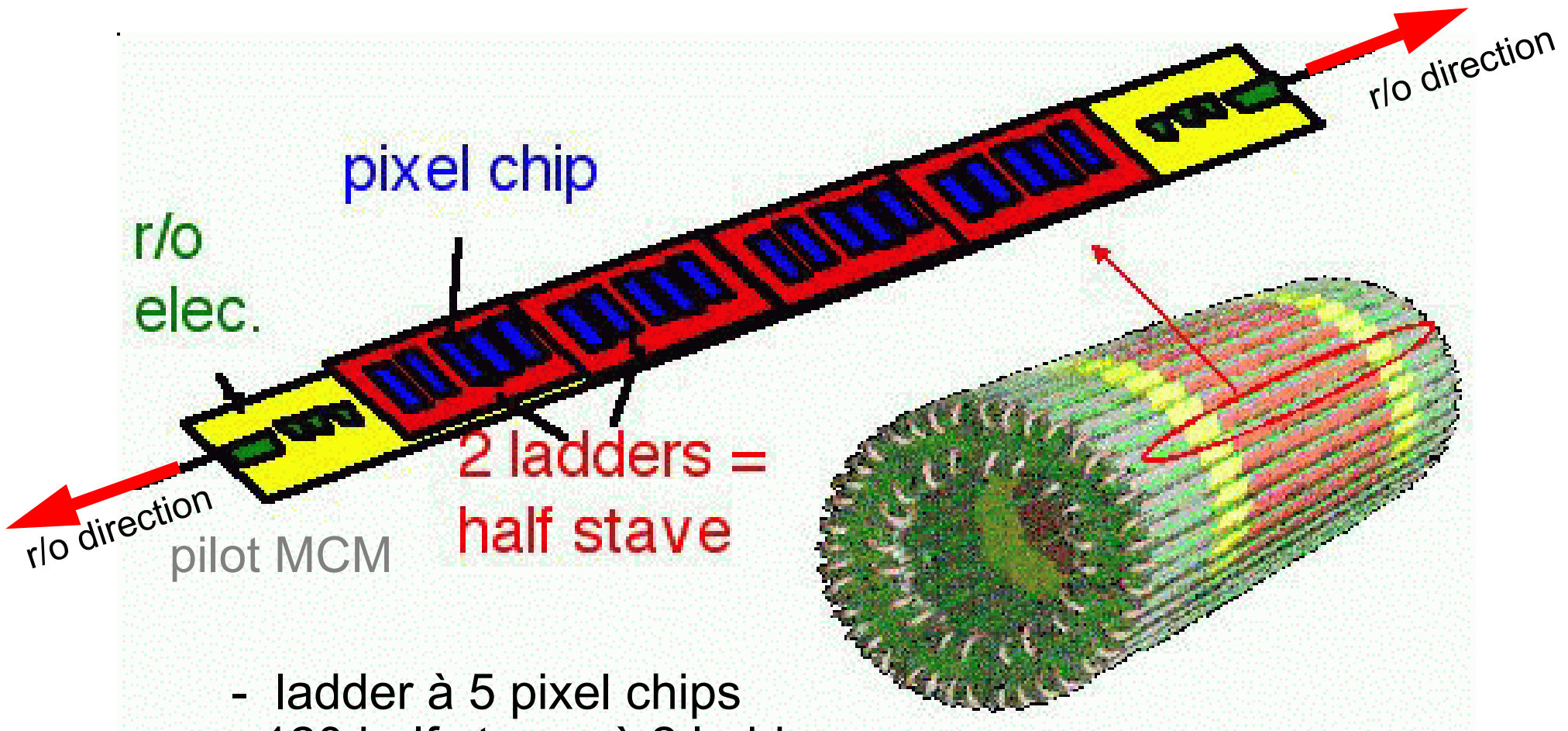
**PHENIX Silicon Upgrades Meeting**  
**10 April 2003**

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*RIKEN - Radiation Laboratory*

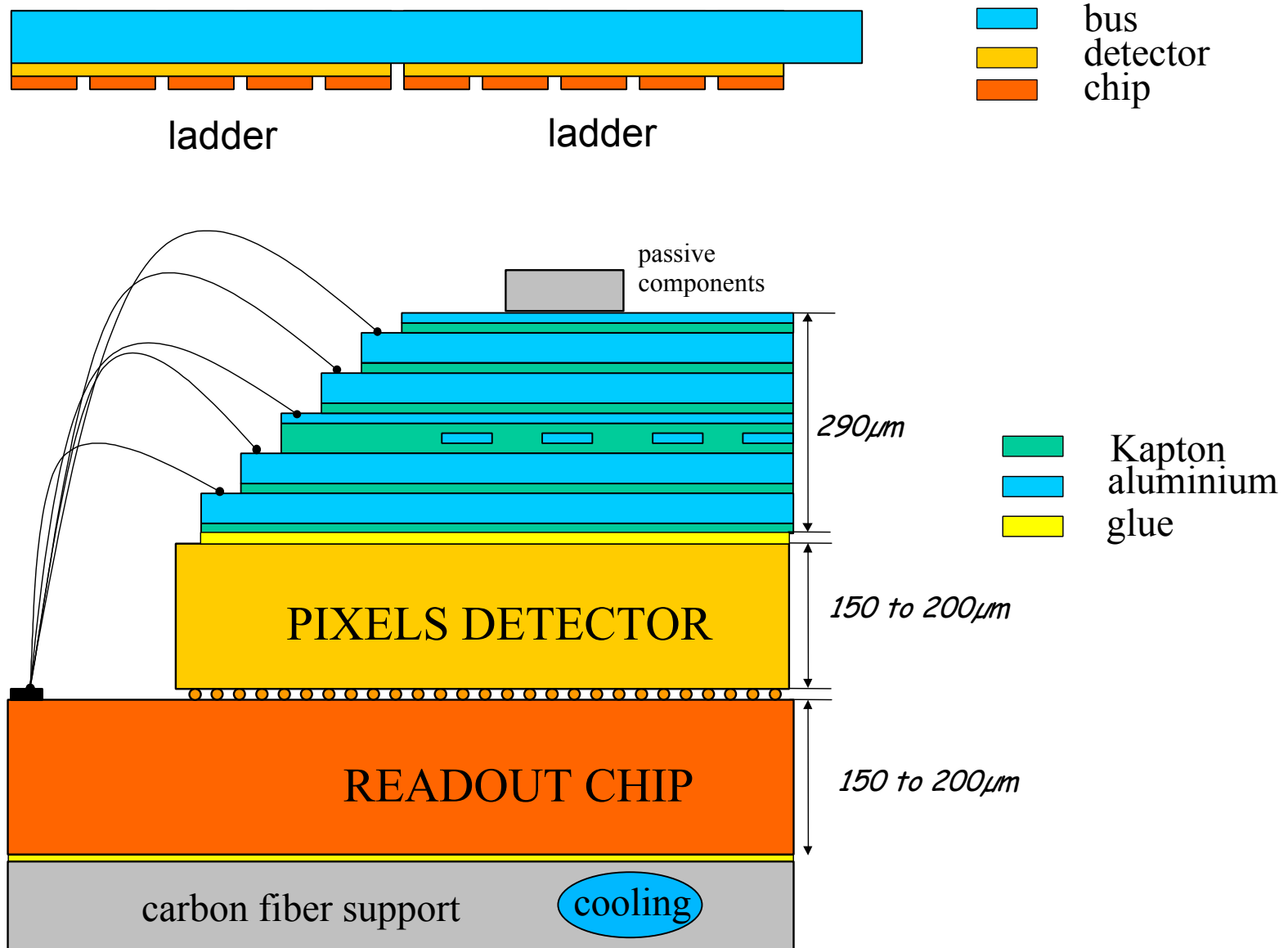


# Brief overview of the ALICE Pixel detector bus/MCM concept

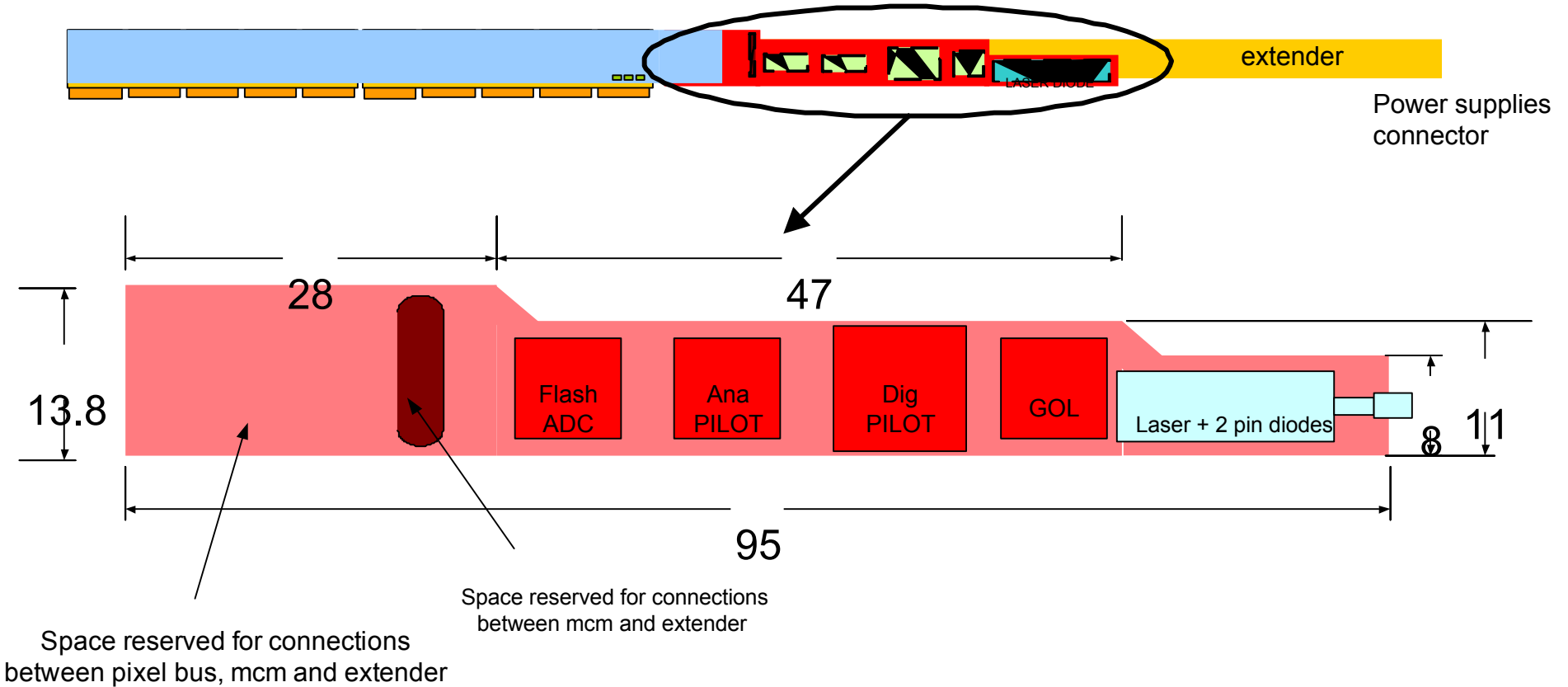


- ladder à 5 pixel chips
- 120 half staves à 2 ladders
- 120 MCMs
- 1200 pixel chips, 10 M pixels total, arranged in 2 barrels

# ALICE Pixel bus



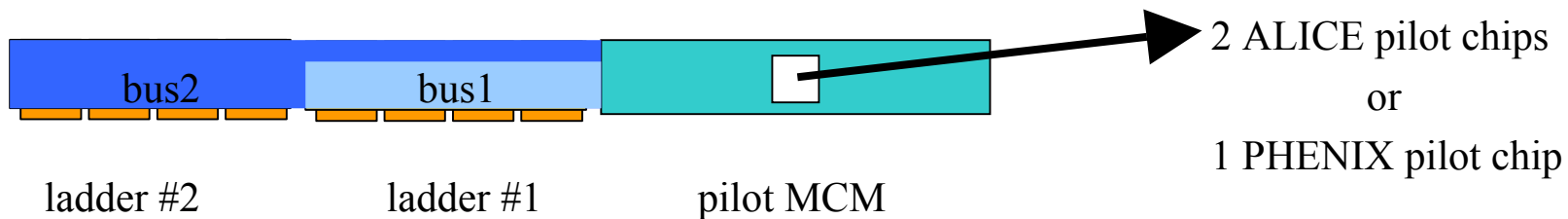
# ALICE Pilot MCM



# RIKEN R&D plans

	ALICE	PHENIX
chips per ladder	5	4
ladders per half stave	2	2
bus per half stave	1	<b>2</b>
pilot chips per half stave	1	<b>2 (1)</b>

→ Increase readout speed, from  $\sim 200 \mu\text{s}$  to  $\sim 100 (80) \mu\text{s}$ .



- \* Develop doubled bus system: 1 separate bus for ladder 1  
1 separate bus for ladder 2
- \* Read every ladder by one pilot chip individually, or develop a new pilot chip (preferred) that can read two busses in parallel.

# RIKEN plans

- Effectively, collaboration effort between RIKEN and ALICE/CERN has started with beginning of JFY2003 (April 1<sup>st</sup>).
- At CERN, three RIKEN persons are now involved in that project:  
Johann Heuser, Hiroyuki Kano, (Hiroaki Ohnishi)
- Next to contributions to the ALICE pixel project at CERN, PHENIX related design work will be done at CERN and in Japan. It is planned to collaborate with industry in Japan on the production of the bus.
- Details will evolve with time and progress made in this project.