

# Preparation of ERT-RICH for RUN9

**K. Utsunomiya, Y. Watanabe**  
**University of Tokyo**

Y. Yamaguchi, T. Gunji, K. Okada,  
K. Ozawa, Y.Hori,  
S.Boose, S.A.Polizzo

# ERT-RICH trigger boards

**We need at least 4 boards for Run9**

**since 4 boards were dead during Run8.**

## RICH trigger boards

List of spare boards (none of them worked during Run8)

#	FLEX 10K	TB check	IR check	Comment	
14	RI208-4	OK	OK (Dec.9)	MAX chip new configuration	
04	RI208-4	OK	-	Hopefully it works.	
32	RC208-4	OK	-		
33	RC208-4	OK	always0	analog power? 30th are different?	
34	RC208-4	OK	-		
30	RC208-4	-	-	Japan	
01	RI208-4	not OK		GLINK chip	
07	RI208-4	not OK		FLEX10K (upper)	
20	RI208-4	not OK		Buffer chip for the control signal	
22	RI208-4	not OK		Buffer chip for the control signal	
09	RI208-4	-	mostly OK	sometimes got quiet, it was installed in WN1.	

We hope we get enough boards by the Run9.

12/10/2008

7

From K.Okada's talk  
Dec. 9, 2008 Detector  
Council Meeting.

Two spare boards work  
well.

We checked FPGA chips, registers, power supplies and so on, on broken and “not-working” spare boards .

# Current status of ERT-RICH boards.

	Dec,2008	Now	
Board-Number	Status	Status	Comment
01	NOT OK	OK	Replaced a GLINK chip.
04	OK	OK	
07	NOT OK	OK	Replaced a FLEX10K (upper) and a regulator for -5V.
09	Mostly OK	Not OK	Some AD converters are broken?
13	-	OK	
14	OK(Dec.9)	OK	
20	NOT OK	OK	Replaced a buffer chip for the control signal
22	NOT OK	OK	
31	NOT OK	OK	Replaced registers which make AD reference voltage.
32	NOT OK	OK	
33	NOT OK	OK	
34	NOT OK	OK	

**Now 11 boards work fine.**

# How to check

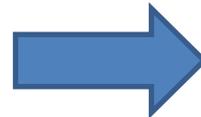
## - Test Bench check

Probing and checking trigger bits at several points on the board, using pseudo-signals.



## - IR check

High threshold(3 p.e)

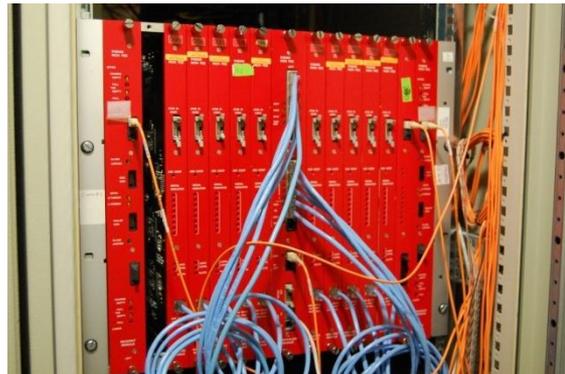


Low threshold

No trigger bit

Trigger bit

**0**

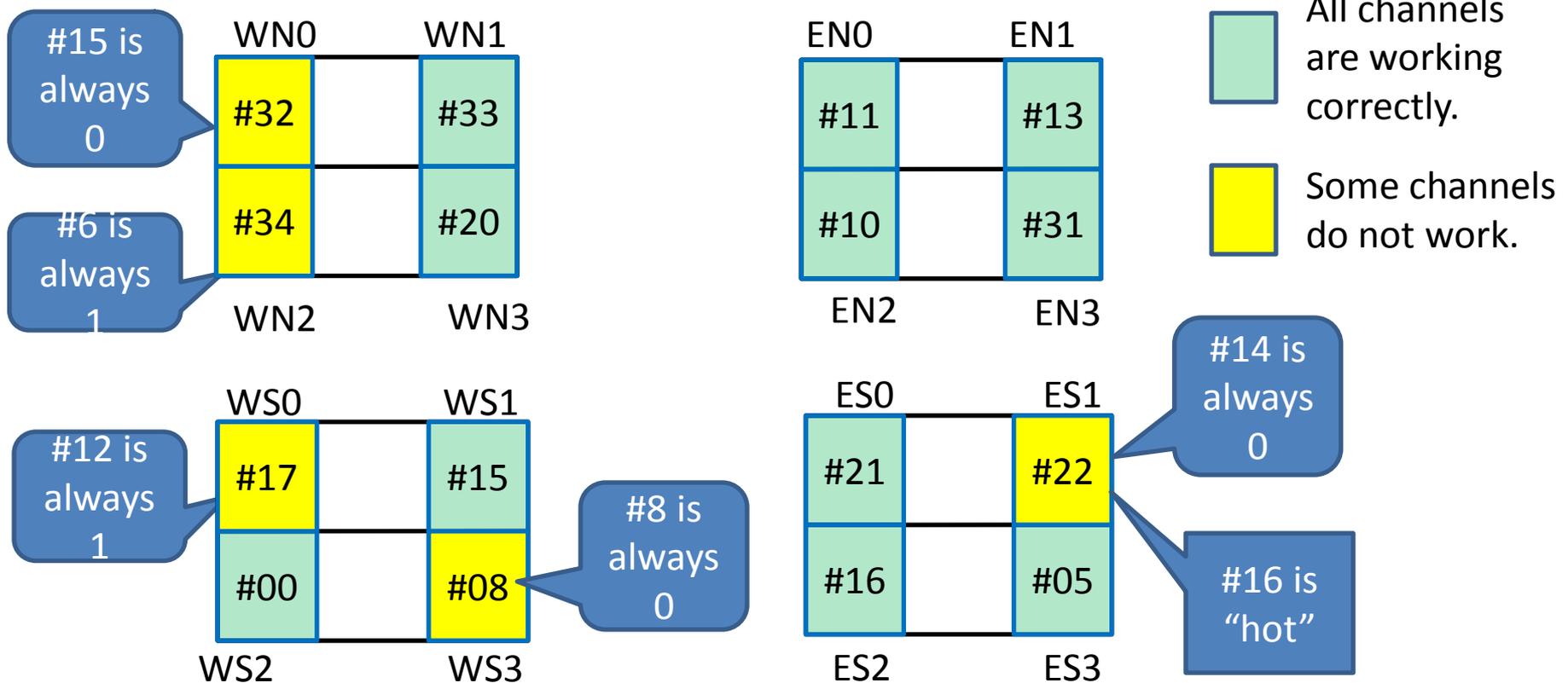


**1**

Triggered by noise

# Current status

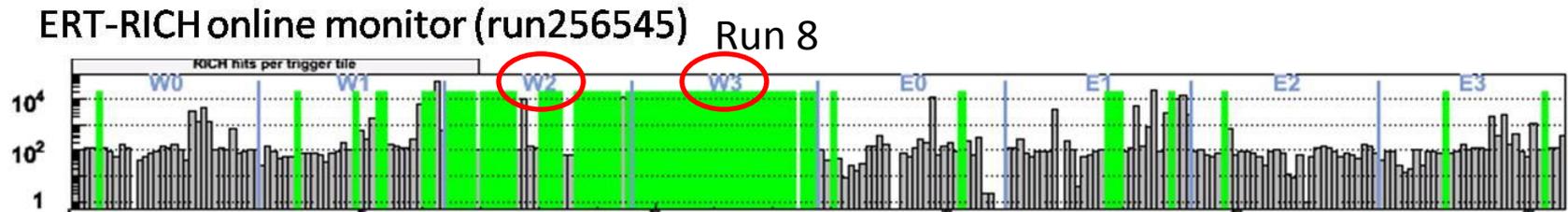
- Each board has 16 channels. 16 boards in total.



- We regard the channel "hot" when it has more than 50% "hot" events
- Even if we inserted another board, the channel always being 0 did not change, so problems are not in the ERT-RICH trigger boards but in the crates.
- We will replace the boards which have a channel always being 1.

# Conclusion

1: **98%** works fine.



4/16 level-1 trigger boards  
were not functioned.



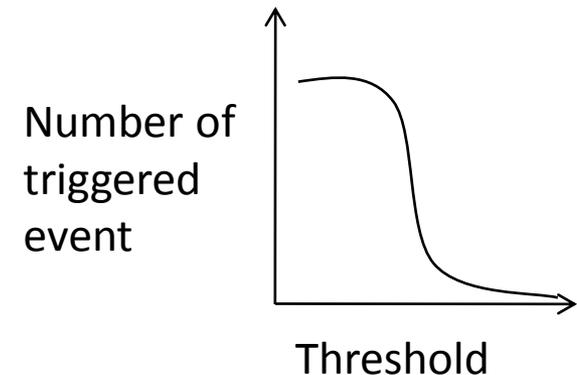
**We can remove some masks on W2 & W3**

2: We have **7** spares.

(#01,#02,#04,#06,#07,#12,#14)

# Future plan

- Check the trigger bits with RICH HV on for various threshold settings (threshold scan/hot tile check)
  - Make a “turn-on-curve”
- Check the response to signal with RICH-LED.
  - Make a “turn-on-curve” plot.
  - We need a partition to take data of ERT and RICH at the same time.



- Check the performance using collision data as soon as possible after the physics run begins.

# Back-Up

# RICH trigger boards

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List of spare boards (none of them worked during Run8) --- (Dec.12,2008)

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22	RI208-4	not OK		Buffer chip for the control signal
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We checked FPGA chips, registers, power supplies and so on, on the other boards .

# How to check in IR

High threshold  Low threshold

No trigger bit

**0**

	NW0	NW1	NW2	NW3
19	0	0	0	0
19	0	0	0	0
19	0	0	0	10
19	0	0	0	130
19	0	0	0	110

Trigger bit

**1**

	NW0	NW1	NW2	NW3
19	fffd	c9e0	ffff	ffff
19	fffd	3e00	ffff	ffb3
19	fffd	ffa7	ffff	ffff
19	fffd	3c00	ffff	ffff
19	fffd	8f00	ffff	dfff