

- R&D issues
 - readout chip decision
 - interface with PHENIX
 - ladder
- Technical options
 - SVX4 or MVD-TGV+AMU/ADC recut
 - other sensors

→ Strip sensor

BNL instrumentation / RIKEN / Kyoto U. Strip readout / Interface with PHENIX BNL / ORNL / RIKEN / Kyoto U.

Strip sensor

- Technical options
 - Zheng Li's sensor or other sensors
- R&D
 - telescope with VA2 readout chip and its beam test ongoing
 - cooling
 - readout chip decision ...
 - interface with PHENIX ...
- Manpower
 - BNL instrumentation / RIKEN / Kyoto U.

Strip sensor readout / Interface with PHENIX

- Technical options
 - SVX4 readout chip or MVD-TGV+AMU/ADC recut
 - data management method ladder structure
 - local processing or driving signals on kapton cables
 - buffering capability
 - low power data transmission
- R&D
 - mismatch of Zheng Li's sensor (DC coupling) and SVX4 chip (AC coupling)
 - accumulation of leakage current frequent reset of the SVX4
 - cooling (lower than the room temperature) to decrease leakage current
 - ladder structure
- Manpower



Hybrid pixel

- Technical options
 - ALICE1 hybrid or other hybrids
 - BTeV FPIX2 readout chip
 - monolithic pixel ...
- R&D
 - readout interface with PHENIX …
 - bump bonding / thinning ...
- Manpower
 - RIKEN
 - collaboration with NA60 / ALICE
 - 2 FTE post-docs at CERN (and 1-2 more will be added)

Bump bonding / Thinning

- Technical options
 - Fermilab-led efforts
 - PHENIX involvement by ISU
 - McNC North Carolina/Unitive
 - AIT Hong-Kong
 - CERN-led efforts
 - PHENIX involvement by RIKEN
- R&D
 - alternative options for bump bonding / thining
 - evaluation of bump-bonding samples made by McNC and AIT
- Manpower
 - R&D proposal
 - 0.5 FTE at post-doc level in FY2003 and FY2004
 - RIKEN
 - collaboration with NA60 / ALICE
 - 2 FTE post-docs at CERN (and 1-2 more will be added)

Monolithic pixel

- Technical options
 - epitaxial monolithic detectors by LEPSI
 - float-zone monolithic detectors by Bonn/Munich
- R&D
 - increased speed of readout
 - R&D started
 - readout time halved to 110 nsec/pixel or 5 $\mu \text{sec/chip}$
 - next steps, event buffering
 - thick, high-quality silicon
 - partner with Munich/Bonn groups to build readout on top of detector-grade silicon
- Manpower
 - R&D proposal
 - 0.5 FTE at post-doc level and 1 FTE master student in FY2003 FY2005

Hybrid pixel readout / Interface with PHENIX

- Technical options
 - ALICE pilot chip or our own pilot chip
 - FEM or FEM+CCB
- R&D
 - parallelization of readout
 - development of FEM (and CCB)
- Manpower
 - R&D proposal
 - RIKEN
 - collaboration is starting with KEK instrumentation



Endcap pixel

- Technical options
- R&D
 - increased capacitance load on the readout chip
 - sensor pad topology
 - routing of control lines
 - location of the pilot chip
- Manpower

Support frame

- Technical options
 - conceptual design by the engineering team that designed the ATLAS support frame (HYTEC)
 - recommendation as to the best technical appoach and the areas that need further study and prototype
- R&D
- Manpower

R&D budget request

- PHENIX institutional involvement
 - Silicon strip
 - BNL (physics, instrumentation), RIKEN, Kyoto U., ORNL
 - Silicon pixel
 - RIKEN, Stony Brook, ISU
 - Endcap pixel
 - LANL
 - Support frame
 - LANL, RIKEN

- Related R&D efforts
 - Hybrid pixel
 - NA60, ALICE
 - Monolithic pixel
 - STAR