EIC Generic Detector R & D Proposal Presentation

Brookhaven National Laboratory
May 9-10, 2011

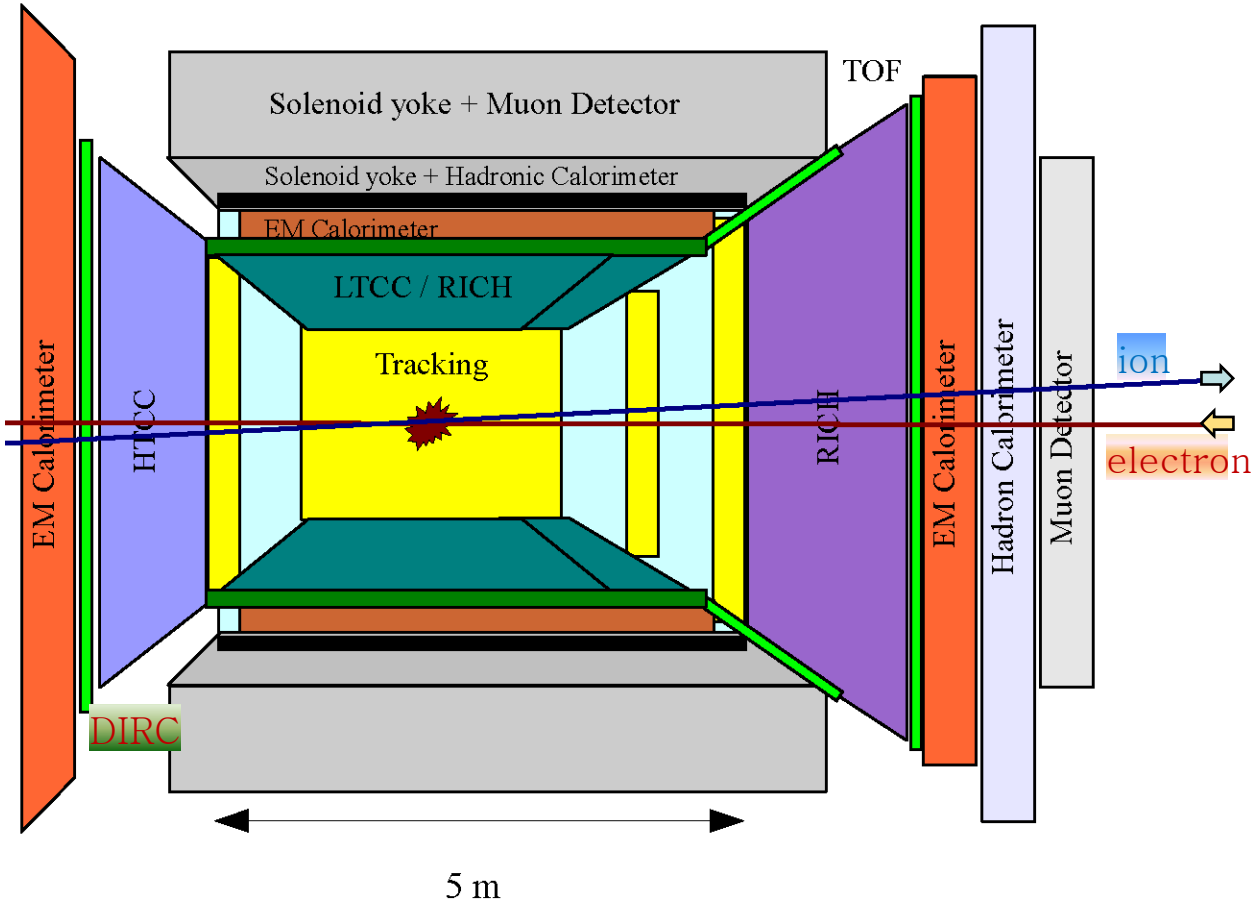
R. Chris Cuevas
Jefferson Lab, Newport News, VA

Outline

- Motivation and Relevance to EIC
  - Detector readout requirements demand sophisticated front-end DAq
  - Immediate need to support detector R&D groups
- Design Approach
  - Block Diagram/Specifications
  - Past experience: "What have we done?"
  - What can be accomplished with modest increments in our present technology/designs?
- R&D Expected Results and Deliverables
- R&D Project Cost & Schedule
- Conclusion

Design Motivation – Relevance to EIC

Consider a "Generic" Top Level Detector System View



- Each detector has a specific electronic device to drive a signal to the DAq system

- Examples:
  - Wire Chamber Pre-Amps
  - Photomultipliers
  - SiPM
  - Custom ASIC for: (Example)
    - Silicon Strip
    - GEM
    - uMegas
    - Pixel

Design Motivation – Relevance to EIC

- Design of the detector electronic devices is not the focus of this presentation

- Those device designs require close collaboration with the detector development groups to ensure the signal rates, dynamic range, timing resolution, charge resolution, gas gains, etc are optimized for the specific detector.

  Example:
  Detector Type: Wire chamber
  Detector Electronics: Sense wire preamplifier
  Preamplifier specifications:
  - Multichannel Large ASIC, or single channel?
  - Gain? (mv/fC)
  - Power?
  - Input rate?
  - Dynamic range?
  - Analog or discriminated output only?

- Other detectors will use proven single anode PMT where timing resolution is critical and larger sections of the detector are combined into one PMT readout.

  Examples:
  Detector Type: High Threshold Cerenkov Counter
  Detector Electronics: PMT with coaxial readout for single anode
  Signal output specifications: Fast rise time, well known gain and pulse shape for MIS

Design Motivation – Relevance to EIC

- About two years ago, a short list of Detector Signal Capture and Trigger System R&D topics was created with projects that Jefferson Lab could contribute to the EIC design efforts.

Detector signal capture & Trigger System

Continue R&D of high speed Flash ADC modules

JLAB design runs at 4nS sampling(250MHz) which is adequate for many detector signal shapes

Commercial ADC chips are available at 2nS(500MHz) and 1nS(1GHz) sampling

Engineering design will be needed to solve cooling issues and board layout challenges

Continue R&D efforts with latest FPGA technology → 500MHz clocking exists now on some devices

Continue R&D efforts to use industry standards: (VXS, or new VPX) for extremely high speed serial transmission for Level 1 trigger decisions and global timing synchronization

Continue R&D of multi-crate DAQ with L1 trigger rates exceeding 150KHz

JLAB *prototype* multi-crate system achieves 165KHz at 80MB/s

Explore the use of high speed serial links as data transfer paths rather than VME backplane method

Continue R&D of Crate Trigger Processor algorithms and Global Trigger hardware designs

Increase International Collaboration group specifically for EIC Readout/DAQ Electronics

R&D for new vertex detector readout chips: Most designs are for much longer bunch crossing time

FPGA design/simulation and firmware code sharing

Detector data rate simulation including trigger rate studies to improve trigger system design

Design Motivation – Relevance to EIC

- Many items on the previous list have been accomplished, but this proposal will help to continue the R&D needed to verify new technology that will interface directly with EIC detector output electronics.

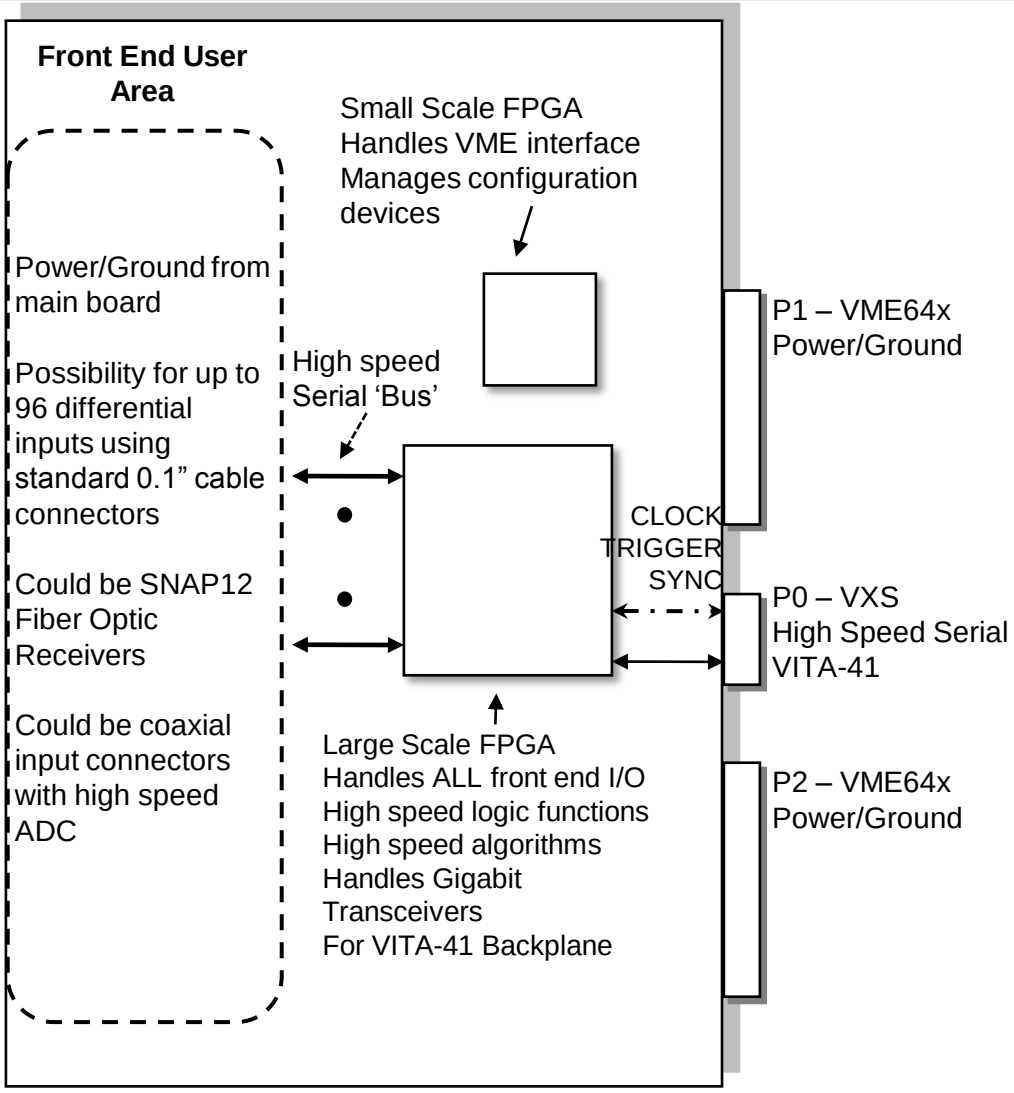
- A flexible front-end module will provide many different detector groups a common method to thoroughly test detector electronic devices such as SiPM, custom ASICs, PMT, WC Pre-amps, etc. during the stages of detector R&D.

- The detector electronic devices will need to be tested to verify that they will meet or exceed the EIC interaction specifications for signal rates, signal dynamic range, timing resolution, charge resolution, and DAq performance.

- The main 'motherboard' would use a standard VXS backplane interface that supports 2eSST readout and allow detector groups to develop firmware for their specific FPGA or custom electronic devices on the detachable front-end mezzanine card.

- The electronic interface description and design between the 'motherboard' and mezzanine card would be freely distributed to all EIC collaborating institutions.

Design Approach – Block Diagram/Specification
Front End Readout Module



9U x 220mm single width VXS "Payload" format

- Front End User Area is a mezzanine card that interfaces to motherboard
- Power, power return, and data interface busses will be fully specified for mezzanine
- Design will allow adequate bandwidth for readout of front-end data via 2eSST on '64x
- Will provide robust proven interface to the VXS backplane fabric to develop custom triggering applications for detector specific designs.
- Front End User Area mezzanine is vendor 'agnostic' and allows designers their choice of FPGA family.
- 9U x 220mm format offers high channel density and circuit design/routing area

Design Approach – Block Diagram/Specification

- Emphasis:
  - Front End User Area will be used to match specifically to a detector output device
  - Ample front panel area to interface and optimize channel density to detector output cabling
  - One motherboard design that would offer a large scale FPGA to manage mezzanine interface and high speed serial Gigabit streams to the VXS fabric.
  - Motherboard design will benefit from existing robust designs used extensively at Jefferson Lab for '64x 2eSST readout and general purpose VME register control

- Specification Comparison:

Parameter	Existing Design	FERM proposal
#of channels (Coax)	16	24
# of Bits/channel	12	10-12
Sample rate	250MHz	250MHz – 500MHz
Fiber Optic transceivers Data input capability	8 - (MTP- 4Tx/4Rx) 80Gb/s	12 Rx- (SNAP12 or Avago Modpac) 360Gb/s
VME2eSST	Yes	Yes
VXS transmission rate Aggregate (8/10b encoded)	2 Rx/Tx at 2.5Gb/s 4Gb/s	4 Rx/Tx at 5Gb/s 16Gb/s
#Channel/Crate(Lemo Coax)	256	384
Flexible input design	No	Yes

Design Approach

- The FERM proposal is a very good example of what can be accomplished with a small upgrade to our existing hardware designs.

- For instance, by selecting the latest FPGA and doubling the serial Transceiver rate, we will be able to increase the output bandwidth for trigger specific applications.

  Examples:

  -- Existing designs transfer 16-bit Energy Sum information every 4ns → 4Gb/s
  By doubling this rate or adding additional serial links, the Energy Sum AND cluster hit counting data can be transferred forward to the global trigger modules.

  -- Existing global trigger module designs use 4Tx-4Rx Fiber Transceivers running at 2.5Gb/s. Simply changing to a new Fiber Transceiver scheme (SNAP-12 or latest Avago) and using the same parallel fiber optic cabling the input data stream bandwidth increases by a factor of three.

  -- We have a Non-Disclosure Agreement with Avago for their latest technology for parallel optical transceivers. Using these devices and increasing the serial rate would be another example of the usefulness of the flexible input mezzanine idea.

Design Approach – Past Experience

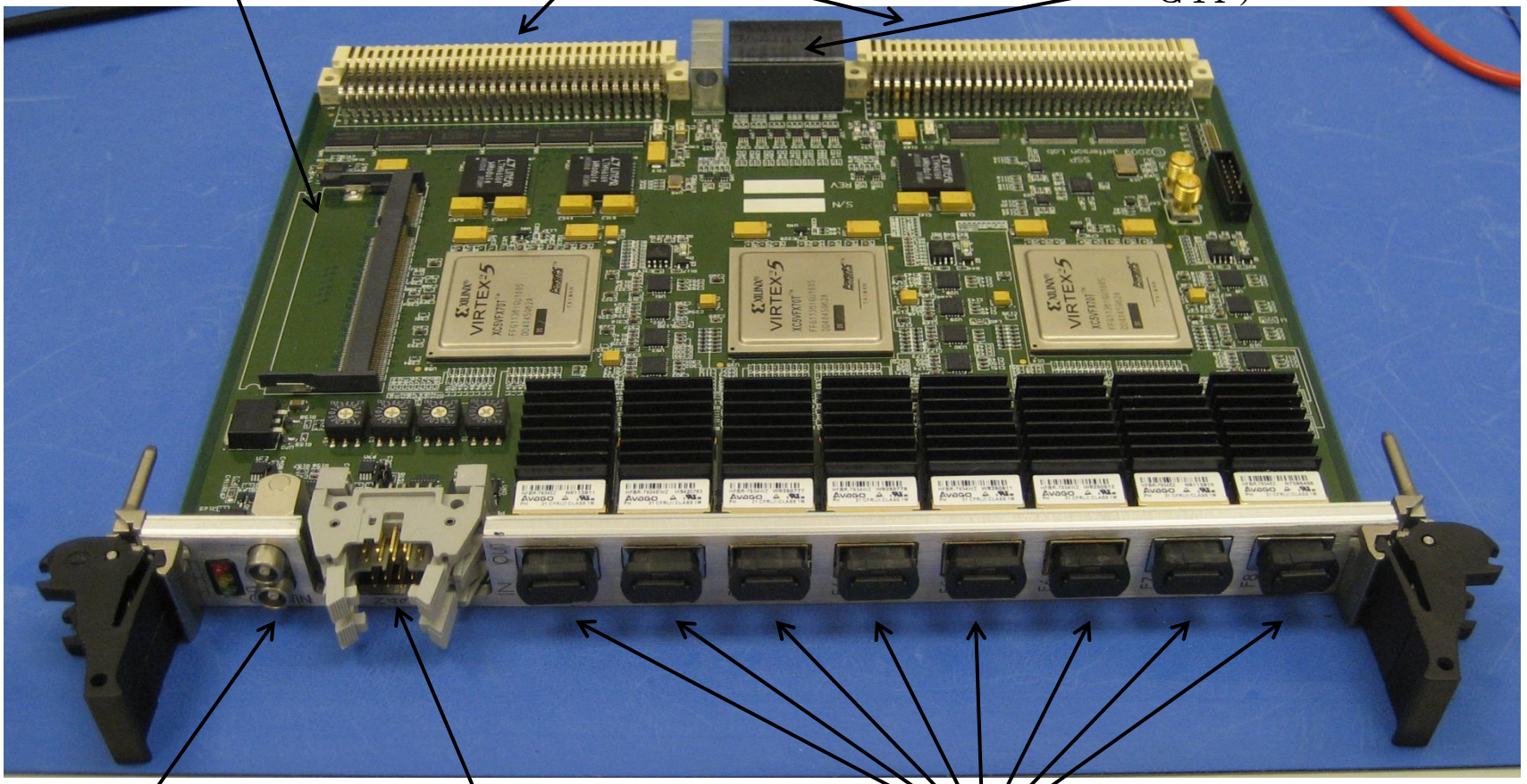
- In the immediate future, detector R&D will require a flexible front-end readout module that will provide detector developers with a well known standard for management of Data Acquisition for analysis of detector performance.

- Implementation of the **F**ront **E**nd **R**eadout **M**odule will be based on our past experience with high speed analog and digital circuit board design for the 6GeV program and recent 12GeV designs. Design capability examples:

  - High-rate capability (200 kHz) from GlueX hadron trigger requirements
  - Advanced algorithms from CLAS12 electron trigger
  - Fully synchronous pipeline DAq system running at 250MHz
  - Multi-Gigabit serial data transmission with new FPGA technology and parallel optics
  - Advanced firmware development tools for Xilinx and Altera FPGA
  - VHDL simulation and verification tools from Aldec and ModelSim
  - Extensive library of CAE/CAD components for schematic capture and PCB design
  - Full implementation of VXS Dual Star (VITA-41) serial backplane fabric
  - Advanced multi-layer circuit board routing tools from Cadence
  - Advanced post layout simulation tools from Mentor Graphics (HyperLynx)

VXS Sub-System Processor

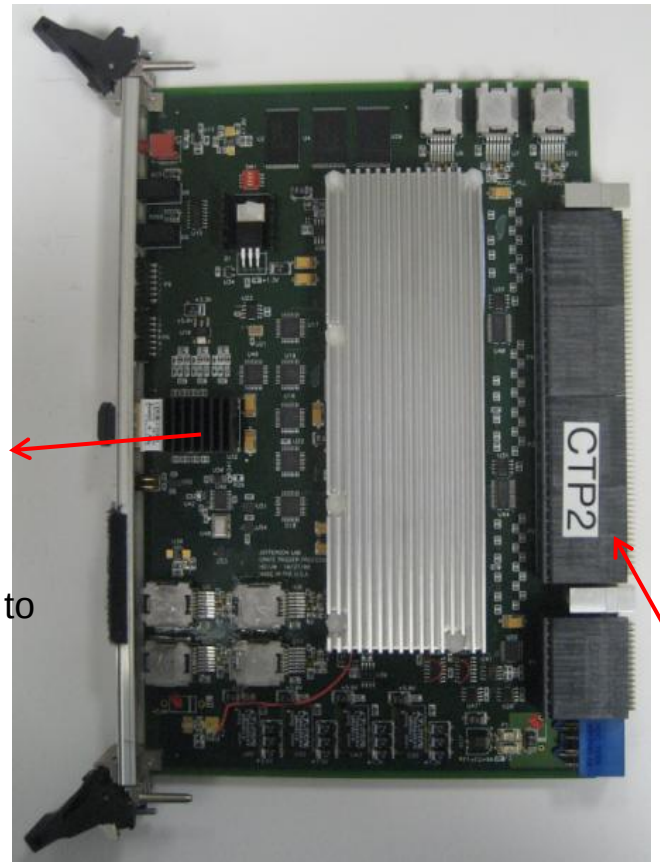
Ben Raydo
9-Sept-2010



Crate Trigger Processor -- VXS Switch Slot

- Includes 3 Xilinx VirtexV FX70T that support 5Gbp/s
- Crate Trigger Processor computes a crate-level energy sum (or hit pattern)
- Computed crate-level value sent via 10Gbps fiber optics to Global Trigger Crate (32bits every 4ns)

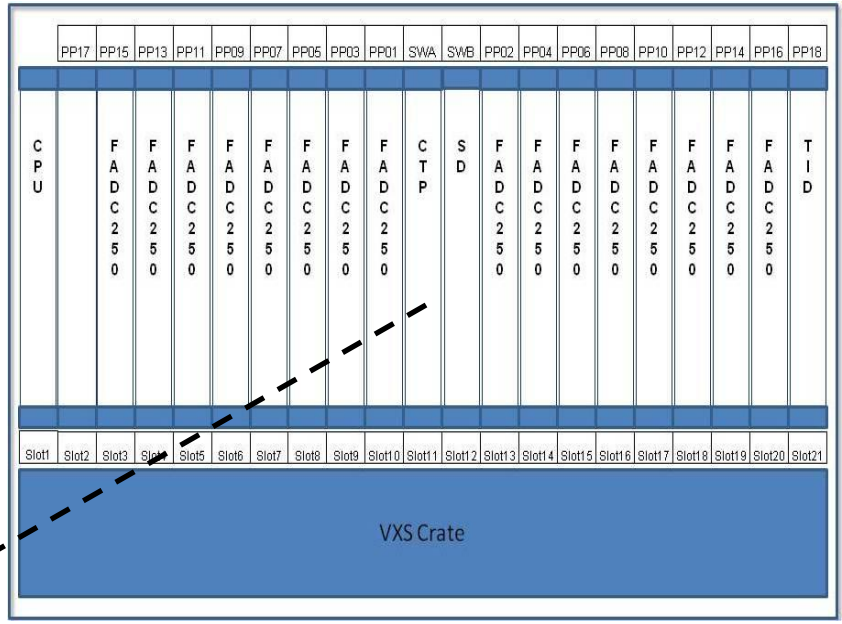
CTP



MTP Parallel Optics

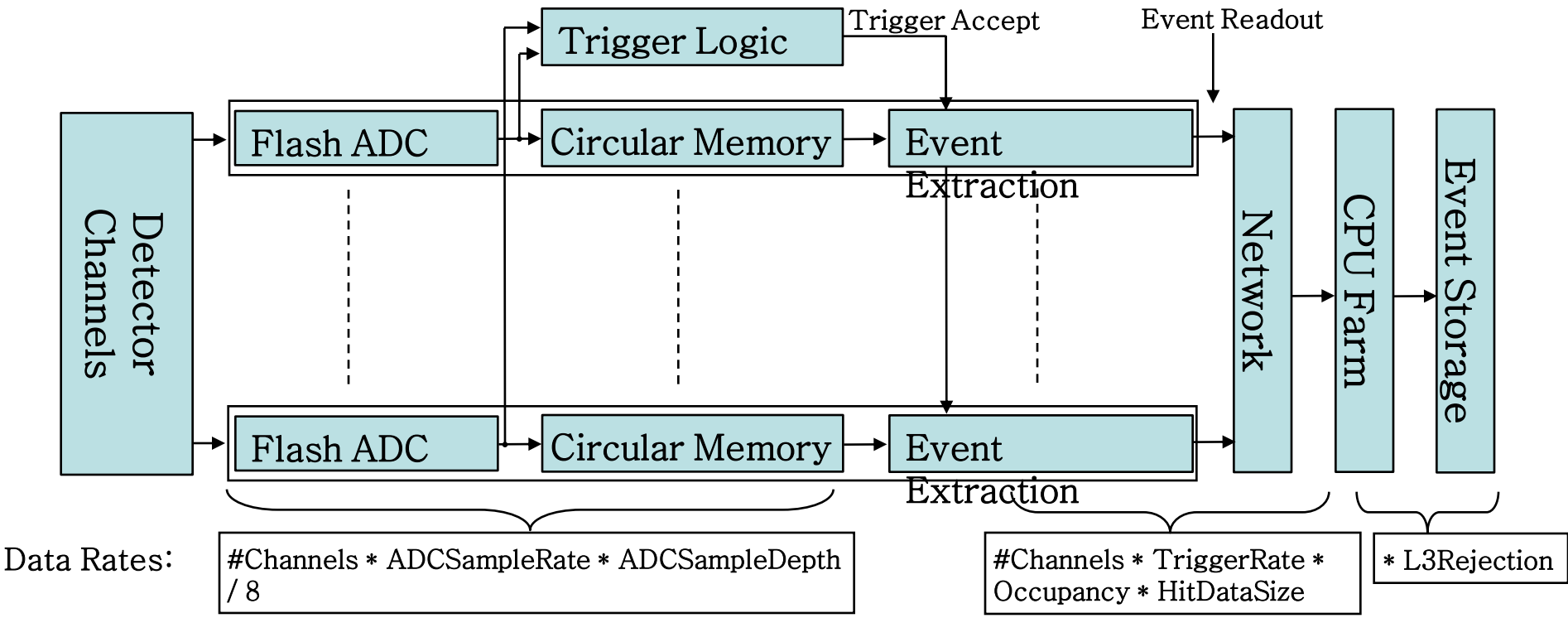
10Gb/s to SSP

VXS Connectors Collect serial data from 16 FADC-250



- Fully populated front end crate for readout of 12GeV detector signals
- 256 coaxial input ‘channels’
- VXS serial fabric is used to transfer trigger information forward to Global Trigger system.

Design Experience -- Pipelined DAQ & Trigger Architecture



- All channels are continuously sampled and stored in a short term circular memory

- Channels participating in trigger send samples to trigger logic. When trigger condition is satisfied, a small region of memory is copied from the circular memory and processed to extract critical pulse details such as timing & energy. **This essentially makes the event size independent of ADC sampling rate, depth, and number of processed points.**

R&D Expected ***Results*** and Deliverables

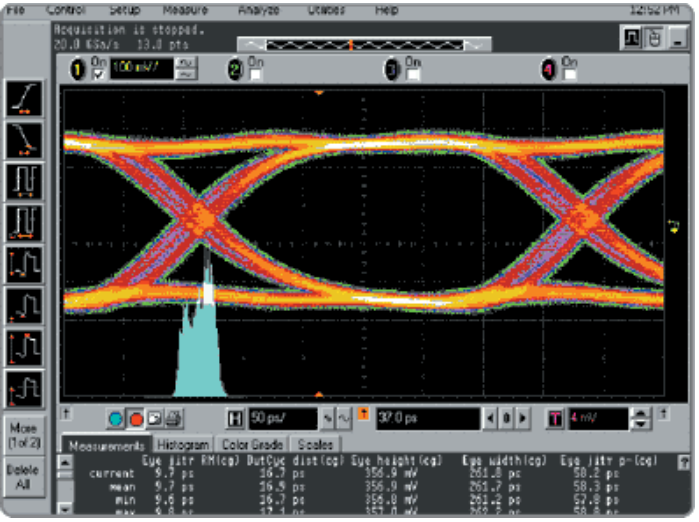
- Extend our engineering experience
- Increase channel density by using a 9U front panel
- Provide a flexible hardware front end design to mate with various detector output signal sources and cabling styles
- Increase existing specifications for serial stream bandwidth on VXS backplane for trigger application development
- Provide a robust, proven interface for 2eSST readout with re-use of existing designs. Detector R&D groups would benefit from a common DAq system.

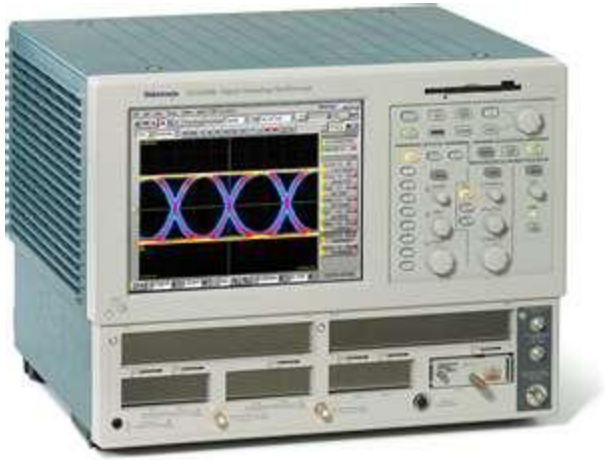
R&D Expected Results and ***Deliverables***

- CAE/CAD design files
- VHDL source and simulation files
- PCB fabrication and assembly files
- Post layout signal integrity analysis files
- Complete Bill Of Materials including mechanical files for front panels and heat sinks
- Thermal analysis and power dissipation analysis
- Full test and measurement documentation of motherboard performance results
- Digital Serial Analysis results for Gigabit Transceivers over VXS backplane

R&D Expected Results and *Deliverables*

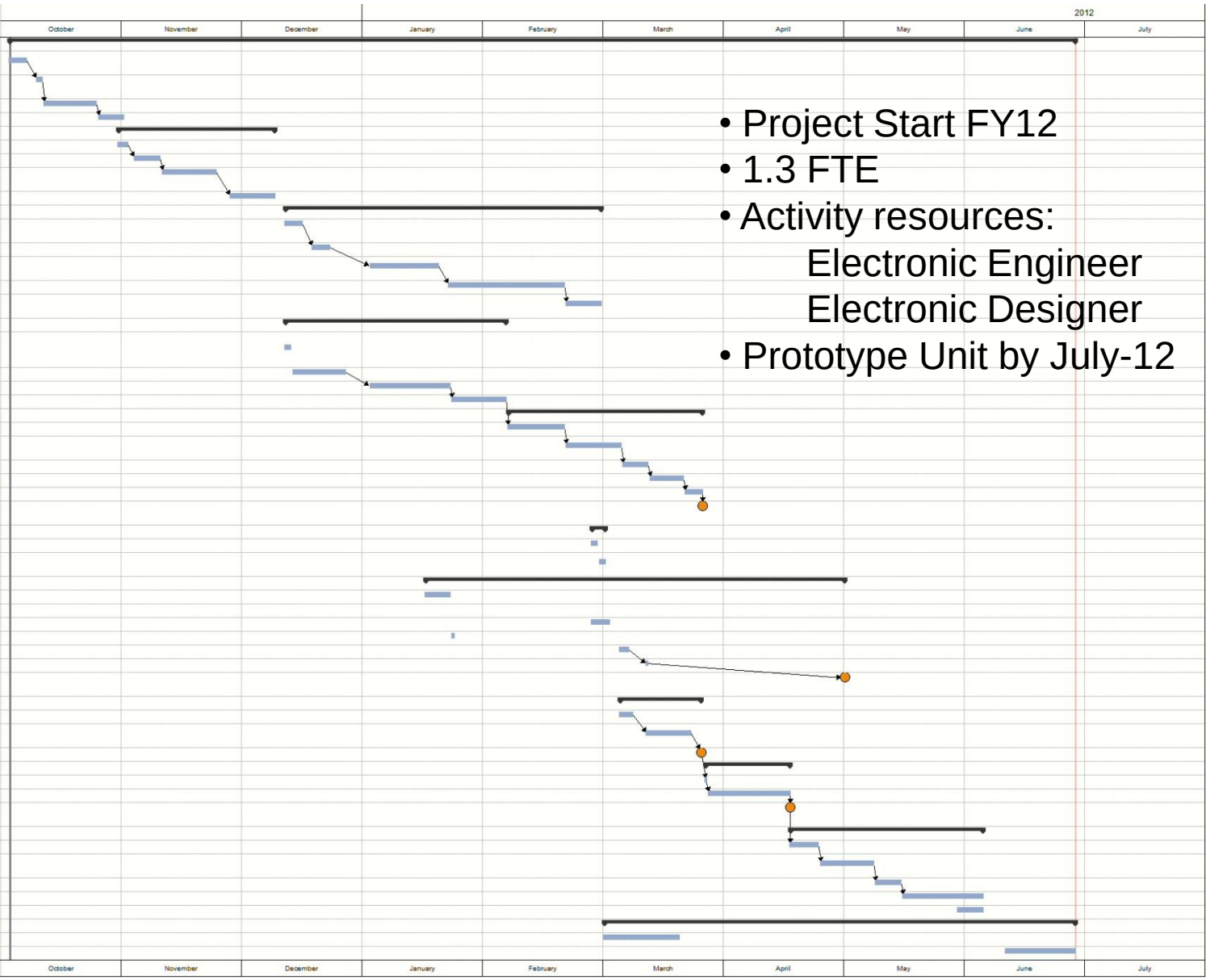
- Proposal request includes new test equipment for high speed serial transceiver measurement and analysis.
- Our existing Digital Serial Analyzer; Tek DSA70000 is adequate for 2.5Gb/s but will need newer model to verify higher speed designs.
- Measuring switching speed Interval Units become critical as serial speed increase (IU @200ps for 5Gb/s) Signal integrity and jitter must be verified for robust designs.





R&D Project Cost & Schedule

	Activity Name	Duration (Work Days)	Resources Assigned	Start Date	Finish Date
1	**WBS 1.0 FERM**	**194.00**		**10/3/11**	**6/28/12**
2	Design Requirements Document.	5.00	EENG	10/3/11	10/7/11
3	Transfer VME/VXS files to Altium	2.00	EDES	10/10/11	10/11/11
4	Component selection	10.00	EENG	10/12/11	10/25/11
5	Build required libraries	5.00	EDES	10/26/11	11/1/11
6	**Design**	**30.00**		**10/31/11**	**12/9/11**
7	9U Motherboard	3.00	EDES	10/31/11	11/2/11
8	VME/VXS section	5.00	EDES, EENG	11/4/11	11/10/11
9	Mezzanine Buss Definition/ Design	10.00	EENG	11/11/11	11/24/11
10	Power Supply Section	10.00	EENG	11/28/11	12/9/11
11	**Firmware**	**58.00**		**12/12/11**	**2/29/12**
12	Design/Re-Use Analysis	5.00	EENG	12/12/11	12/16/11
13	VME/VXS block	5.00	EENG	12/19/11	12/23/11
14	Mezzanine Buss Structure	14.00	EENG	1/3/12	1/20/12
15	VHDL Code	21.00	EENG	1/23/12	2/20/12
16	VHDL simulation/verification	7.00	EENG	2/21/12	2/29/12
17	**Schematic Capture**	**41.00**		**12/12/11**	**2/6/12**
18	VME/VXS interface (Copy from existing designs)	2.00	EDES	12/12/11	12/13/11
19	Motherboard FPGAs	10.00	EDES	12/14/11	12/27/11
20	Mezzanine Interface	15.00	EDES	1/3/12	1/23/12
21	Power Supply sections	10.00	EDES	1/24/12	2/6/12
22	**Board Layout**	**35.00**		**2/7/12**	**3/26/12**
23	Motherboard	10.00	EDES, EENG	2/7/12	2/20/12
24	Mezzanine Buss and interface	10.00	EENG	2/21/12	3/5/12
25	Power Section	5.00	EDES	3/6/12	3/12/12
26	Optimize Pin Swapping	7.00		3/13/12	3/21/12
27	Check PCB files	3.00	EDES, EENG	3/22/12	3/26/12
28	Check manufacturing files	0.00	EDES, EENG	3/26/12	3/26/12
29	**Mechanical**	**4.00**		**2/27/12**	**3/1/12**
30	Front Panel	2.00	EDES	2/27/12	2/28/12
31	Heat Sink or other Hardware	2.00	EDES	2/29/12	3/1/12
32	**Procurements**	**75.00**		**1/17/12**	**5/1/12**
33	Order components	5.00	ADMIN	1/17/12	1/23/12
34	*Receive Components*				
35	Organize Assembly 'Kit'	5.00	ADMIN	2/27/12	3/2/12
36	Order Mechanical Parts	1.00	EDES	1/24/12	1/24/12
37	Specify DSA equipment	3.00	EENG	3/5/12	3/7/12
38	Order DSA equipment	1.00	EENG	3/12/12	3/12/12
39	Receive DSA equipment	0.00		5/1/12	5/1/12
40	**Manufacturing**	**15.00**		**3/5/12**	**3/26/12**
41	Order Circuit Board	4.00	EDES	3/5/12	3/8/12
42	Circuit Board Manufacturing	10.00	Vendor	3/12/12	3/23/12
43	Receive Circuit Board	0.00		3/26/12	3/26/12
44	**Assembly**	**16.00**		**3/27/12**	**4/17/12**
45	Send to Assembly	1.00	EDES	3/27/12	3/27/12
46	Board Solder/Cleaning	15.00	Vendor	3/28/12	4/17/12
47	Receive Board Assembly	0.00		4/17/12	4/17/12
48	**Testing (Functional)**	**35.00**		**4/17/12**	**6/5/12**
49	Power Section Test	5.00	EDES	4/17/12	4/24/12
50	VME/VXS and Mezzanine Bus section	10.00	EENG	4/25/12	5/8/12
51	Data Transfer	5.00	EENG	5/9/12	5/15/12
52	FPGA Processing	15.00	EENG	5/16/12	6/5/12
53	Thermal Analysis	5.00	EENG	5/30/12	6/5/12
54	**Documentation**	**86.00**		**3/1/12**	**6/28/12**
55	User's Manual	14.00	EENG	3/1/12	3/20/12
56	Test Results	14.00	EENG	6/11/12	6/28/12



- Project Start FY12
- 1.3 FTE
- Activity resources:
  - Electronic Engineer
  - Electronic Designer
- Prototype Unit by July-12

R&D Project Cost & Schedule

- Original proposal listed two year approach
  - After review, several steps would be reduced based on re-use of existing schematics and other CAE/CAD files and VHDL code blocks.
- Table below shows complete project cost and includes:
  - Overhead rate
  - Prototype components and board fabrication/assembly
  - Test Equipment

	EENG	EDES	SUM
Total (Days)	182	93	275
FTE	0.83	0.42	1.25
Rate/Year	$95,000	$65,000	
Direct$	$78,591	$27,477	$106,068
G & A (42%)	$33,008	$11,540	$44,549
Total Labor			$150,617
Prototype			$10,000
TEST_EQUIP			$75,000
Project SUM			$235,617

In Conclusion…

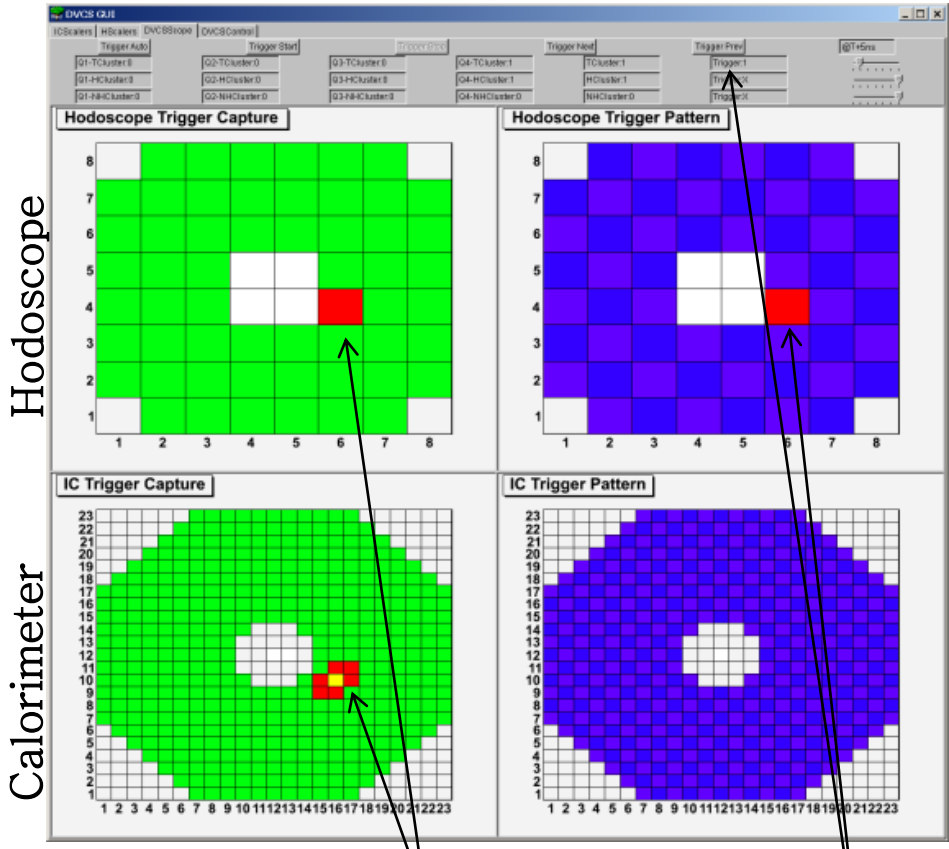
- Detector R&D groups will require front end DAq hardware for testing detector performance.
- A **F**ront **E**nd **R**eadout **M**odule would provide a user defined circuit area to interface specific detector electronic devices. Examples:
  - -- ASIC data output
  - -- Calorimeter PMT or SiPM output (Coax)
  - -- Fiber Optic Transceiver output
- The F.E.R.M. proposal builds on previous experience at Jefferson Lab with pipeline DAq and Trigger systems for both 6GeV and 12GeV experimental programs
- Promotes continuous improvement and collaboration for solving EIC DAq challenges
- Significant section of proposed hardware design is essentially complete.
- Schedule is based on other complex DAq circuit board designs at Jlab
  - -- Test equipment request (purchase) could occur earlier than proposed
  - -- Start in FY12 makes sense because several board designs for 12GeV will be in production so EE resource available

Backup Information

5.3 IC Cluster Finding Trigger

424 Tower $PbWO_4$ Calorimeter & 56 Channel Hodoscope

- FPGA based trigger finds all clusters with calorimeter by considering all possible views with a 3x3 window
- Cluster decisions can optionally be geometrically matched with hodoscope
- Decision time ~85ns, 66MHz pipeline
- Trigger module has a parallel diagnostic trigger that allows arbitrary triggers to be setup for algorithm/channel/timing verification (does not interfere with data taking)



Capturing the Pulses…

Existing System:

Expensive, bulky delay cable dispersive & attenuates

Non-pipelined electronics guarantee dead-time (conversion time)

Gate

Delay line

detector signal

Splitter

QDC

Discriminator

TDC

to primitive trigger logic

Very limited channel resolution used in trigger

multiple modules for time & energy

New System:

(for timing >500ps)

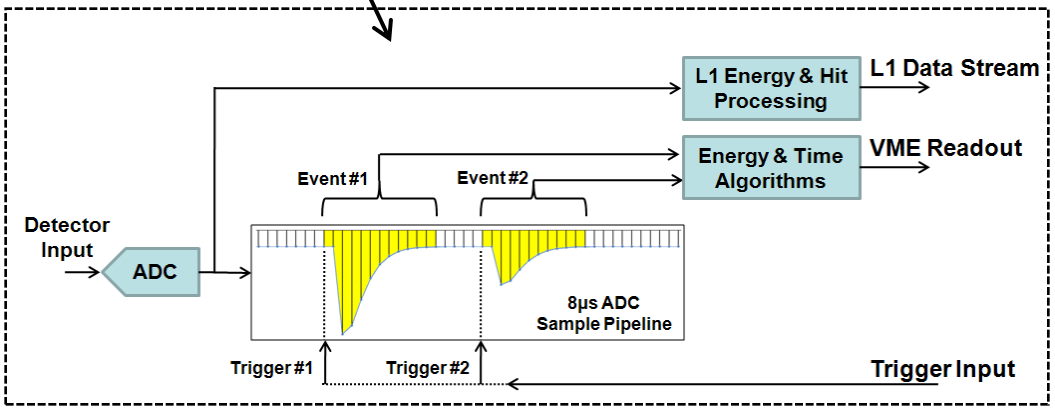
CLAS TOF has >150,000ft delay line!

detector signal

FADC250

to smart trigger logic

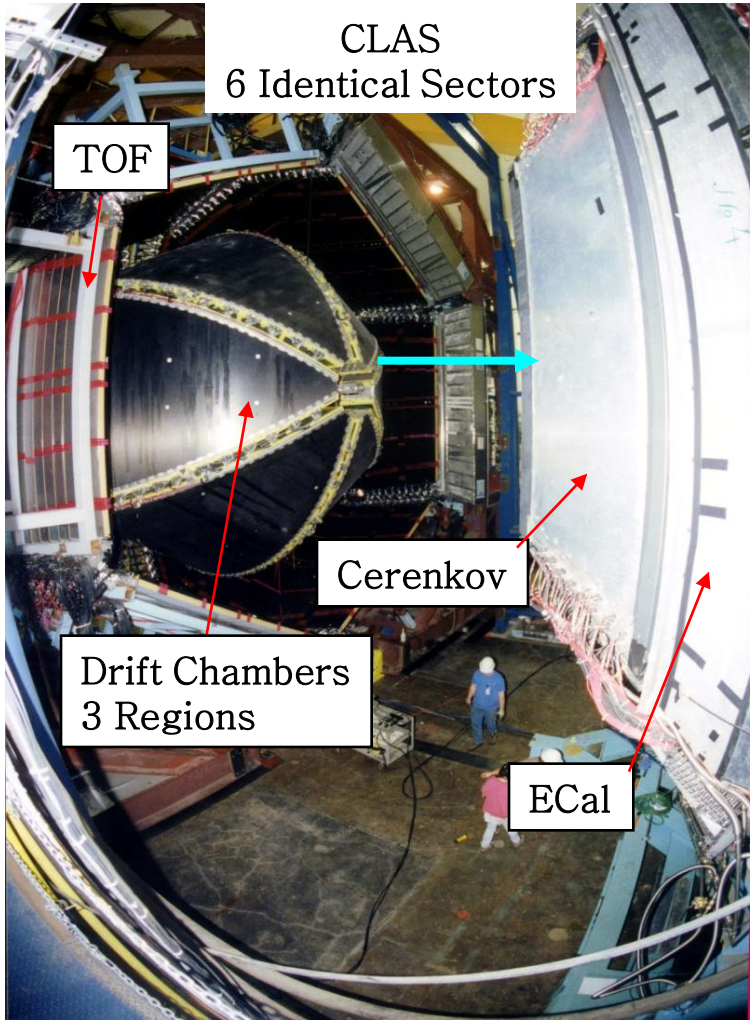
Time, energy, trigger output in 1 module



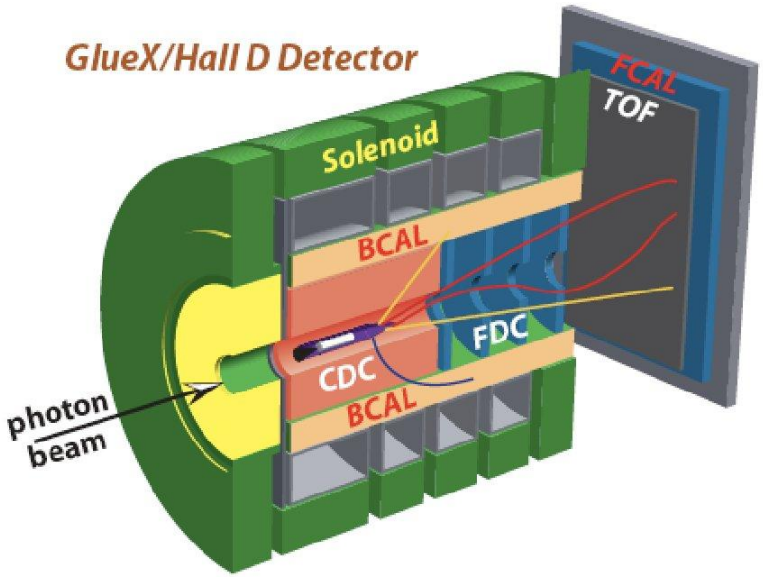
- Pipelined sampling, readout, & trigger -> no dead-time
- Digitization retains original signal integrity
- Long pipeline allow more time for complex triggers

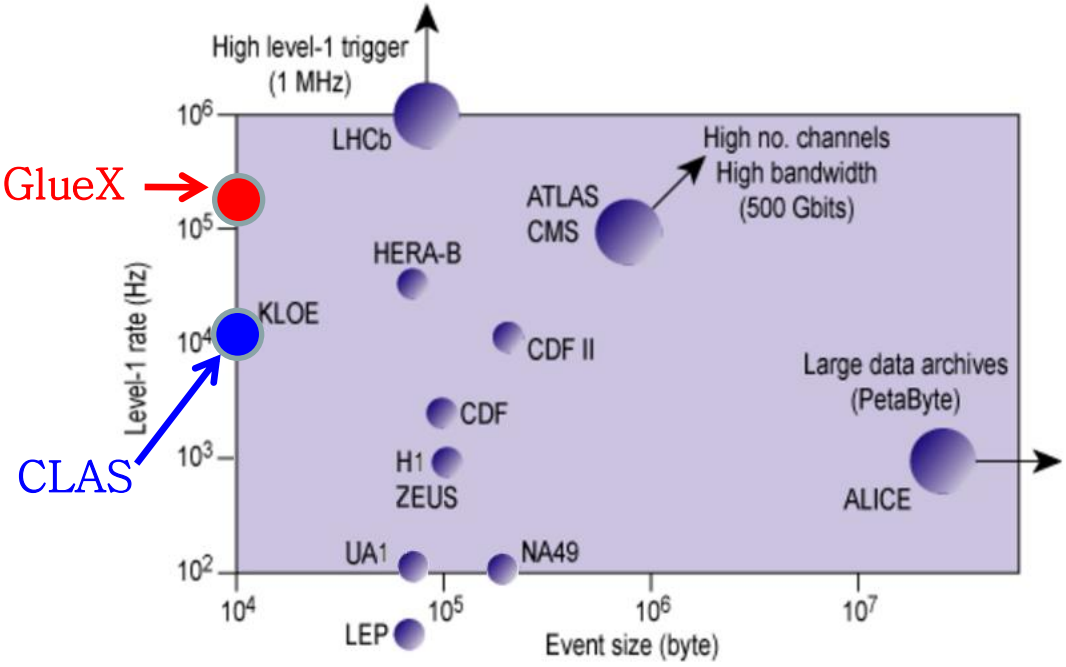
5.1 CLAS Detector & Trigger

- Photon & Electron Experiments with polarized targets, polarized beam
- High Luminosities a few x10^{34}cm^{-2}s^{-1}:
- DAQ event rate designed to ~10KHz
- FPGA based Level 1 Hardware
  - Pipeline design, Dead-timeless, (5ns pipeline clock)
  - Low latency (~150ns)
- Fast Level 1 for ADC Gate, TDC Start
  - TOF, Cerenkov, Electromagnetic Calorimeter
  - Pattern recognition programming
  - Sector based logic for L1 trigger 'equations'
  - Cluster finding for Inner Calorimeter
- Up to 32 Front End ROCs
  - Fastbus, VME, [TDC; ADC; Scalers]



Comparison to CLAS12 (Hall B)





	Hall D–GlueX	Hall B–CLAS
Channel Count:	~20k	~40k
Event Size:	~15kB	~6kB
L1 Rate:	200kHz	10kHz
L1 Data:	3GB/s	60MB/s
To Disk:	L3, 20kHz, 300MB/s	L2, 10kHz, 60MB/s

4.0 Forming Triggers

Rate = L x σ_T ~ 100kHz for EIC@JLab

- Bunch crossing rate of 1.5GHz and Interaction rate of ~100khz we get an **e-p interaction of interest every ~10^4 bunch crossings**
- A trigger occurs when trigger condition is satisfied, which is computed asynchronously with bunch crossing.
- As in CLAS, the time reference is provided by tracking the electron (stable β=1 particle)

Hardware Triggering Options

Background suppression achieved by using advanced triggers:

- Calorimeter cluster finding (sliding window, cluster size & energy)
- Track reconstruction (Shift/sum methods, Hough transform, vertex finding)
- Geometrical matching between detectors

JLab is experienced in these types of trigger designs (6GeV and 12GeV trigger designs)

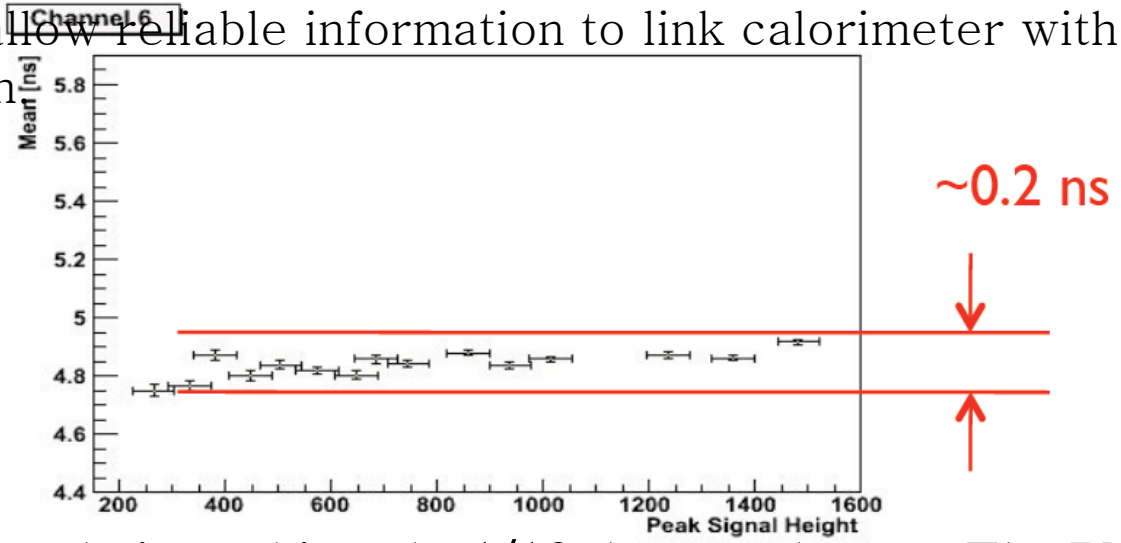
3.5 FADC Sampling – Timing Accuracy

Hall D FCAL PMT: FEU 84-3

- Timing algorithm developed & tested by Indiana University for the Hall D forward calorimeter.

- Implemented on the JLab FADC250 hardware achieving <300ps timing resolution on 50% pulse crossing time with varied signal heights.

- Resolution allow reliable information to link calorimeter with tagged electron bunch



Typical timing resolution achieved ~1/10 the sample rate. The PMT shape will drive the ADC sample rate & depth requirements. From: GlueX Doc# 1258-v1

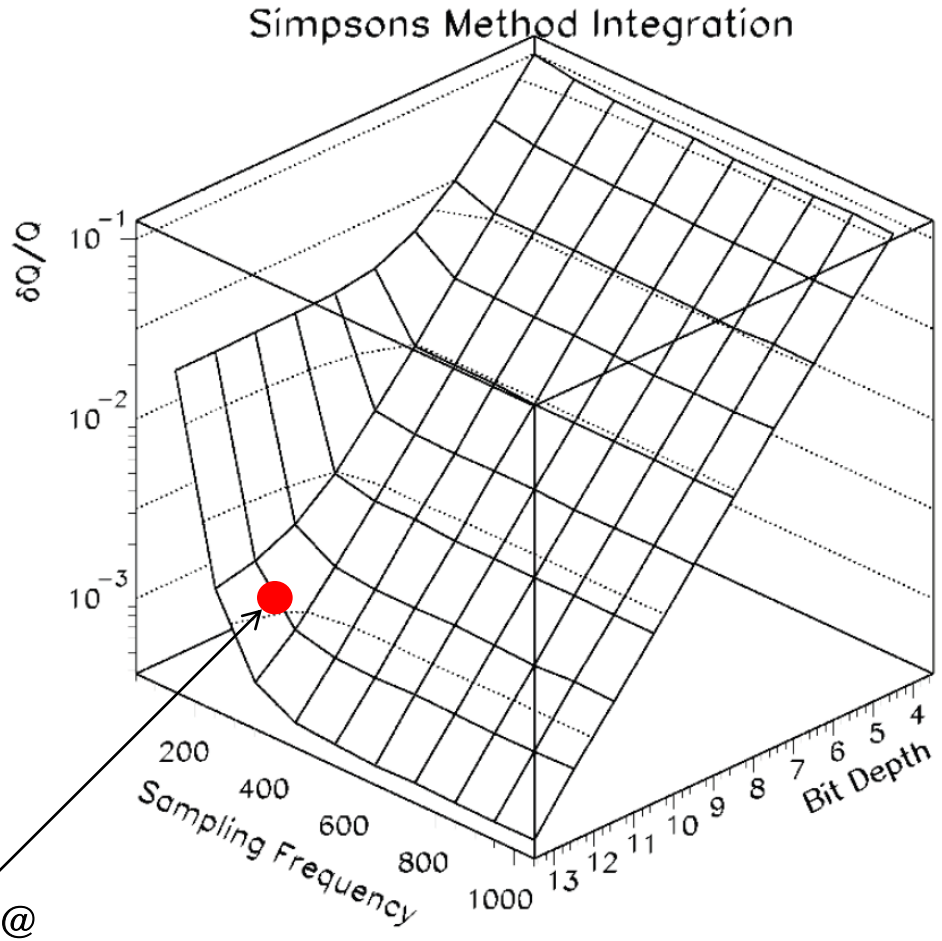
3.4 FADC Sampling – Charge Accuracy

Hall D FCAL PMT: FEU 84-3

-10,000 Random height pulses 10-90% full scale of ADC range simulated

- Sampling frequency makes little difference beyond 250MHz at 12bit, providing ~0.1% charge resolution

- PMT pulse shape dominates sample frequency and bit depth of ADC



250MHz @ 12bit

From: 27 Doc# 425-v1