

Experimental Impact Statement for Installation of an FPGA Radiation Upset Experiment in the PHENIX Interaction Region for RHIC Run-7

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Purpose

In order to test current commercially available FPGA devices for possible use in on-detector electronics in the PHENIX experiment it is necessary to characterize the behavior of these devices in a radiation environment. Devices that use SRAM storage elements (such as Xilinx) are susceptible to alteration of their programming through interactions of radiation within the device. Newer devices that use Flash based memory technology (such as Actel) are reportedly less susceptible to this form of upset in general, however, they may be more susceptible to neutron-induced upsets.

Previous testing in the PHENIX IR using Xilinx rad-hard devices during Run-4 was very successful and resulted in an ISU M.S. Thesis for Steve Skutnik. Interested readers may find a complete description of this work at:

<http://shepody.physics.iastate.edu/skutnik/thesis.pdf>

In this current round of testing, we plan to expand our examination of these devices in two ways. First, we plan to test commercial-grade devices based on both SRAM and Flash technology in the same test setup. Second, we plan to run a prototype readout program and capture the data output to search for transient upsets in the state of internal flip-flops. These upsets do not necessarily cause the device to malfunction, but will result in incorrect data being passed up from the device.

Description of the Experiment

The experiment itself consists of a self-contained box with the two test boards and FPGA's (Xilinx and Actel), Actel and Xilinx USB interface connections, and a parallel to USB I/O interface, (see Figure 1). The box dimensions are 17" x 10" x 3.5". The services required by the box in order to function are +5V and +9V power and three USB connections. The power lines are fused internally in the box with 2A slow-blow fuses.



Figure 1: The FPGA test box, with the cover open, showing the FPGA test boards, USB hub, and digital I/O interface. In the final version of the box the USB hub will be external and connected to the box by three 15-foot USB cables.



Figure 2: The back of the FPGA test box, showing the AC input, CAT5 input, and (external) AC-DC power converters. The external AC-DC converters have been removed and the box requires on +5V and +9V DC low voltage inputs.

The three USB cables coming from the box are ~15 feet in length. These will connect to a USB hub and a USB->Cat5e extender box. Both the USB hub and USB extender will require AC power to operate. We are assuming that 15 feet will be sufficient to locate the hub and extender in a rack or enclosure where AC power is available. The extender has a maximum range of 150 feet of Cat5 cable, which should be sufficient to reach from the PHENIX IR to the rack room, where it will connect to a laptop containing the analysis and configuration software. (The laptop will require network access, and will comply fully with all BNL cybersecurity requirements.)

The running experiment will consist of monitoring the FPGA chip readback and data readout for errors and re-configuring the devices as necessary. Errors will be recorded and correlated with integrated luminosity (BBC and ZDC counts) so that an error rate (per collision) can be determined.

The test box will also be equipped with a set of small radiation dosimetry devices that will be attached to the external surface of the box. We intend that these devices should integrate over one entire running period (heavy ions and/or pp), and we would like to replace them between running periods. Because of this, it would be advantageous if the box were installed so that monitoring devices would be replaced on or very near to the experimental test box.

We would like to install the box prior to the start of Run-7 and leave the box in place throughout the entire run. Radiation induced upsets are rare, so we would like to integrate as much luminosity as possible.

Placement of the Test Box In PHENIX

We currently require some assistance from PHENIX in identifying a candidate location for the FPGA test box.

Because SEU events are relatively rare, we would like to expose the apparatus to as high a particle flux as possible. However, the box represents a substantial amount of material and it would be unacceptable to place the box within the acceptance of the central arms. We would consider placement within one of the muon arms, near or on the central magnet pole, to be optimal. While this would expose the box to a substantial particle flux, as well as neutrons resulting from interactions in the magnet iron, the additional material of the box itself would be insignificant in the muon arms. This also has the added benefit that results from this study may be useful in making decisions regarding the RPC detector electronic for the PHENIX Muon Trigger Upgrade.

PHENIX Resources Required

It is assumed that the services of one PHENIX technician will be required in order to install and remove the test box. The time required will depend on the installation location, but we assume that once physical access is available to the box installation or removal

should take no more than one hour. ISU personnel should be able to handle installation of the extender cable, with guidance from 1008 personnel.

In order to have total control over resetting the various components in the box we would like to have remote control over the LV power to the box, so that it can be cycled remotely from the counting house without making an experimental access. We do not anticipate requiring control over power cycling the USB hub and extender module.

The running of the experimental setup will be done by ISU personnel and will have no impact on and require no support by 1008 personnel.