

## Si R&D Budget Sent to BNL \$ before 40% Overhead

Description	FY03	FY04	FY05
post-doc	60K	60K	30K
Elec. Engineer	175K	175K	100K
Mech. Engineer	50K	100K	50K
Mech. Designer	20K	40K	-
Wafer Fabrication	20K	40K	40K
Prototype fabrication	40K	60K	
Equipment	20K	-	-
<b>Totals</b>	<b>385K</b>	<b>475K</b>	<b>220K</b>



## “Possible Split” be4 Overhead

	FY03	FY04	FY05
Si strip readout, interface with PHENIX	Elect. Engineer	75K	
Hybrid Pixel readout, interface with PHENIX	Elect. Engineer	75K	75K
	Equipment	20K	-
Thinning/Bump	Post-doc	30K	30K
	Wafer Fab	10K	15K
Endcap hybrids	Elec. Engineer		75K
	Wafer Fab		15K
Monolithic	Post-Doc	30K	30K
	Elec. Engineer	25K	25K
	Wafer Fab	10K	10K
Support Frame	Mech. Engineer	50K	100K
	Mech Designer	20K	40K
	Fabrication	40K	60K
	<b>Totals</b>	<b>385K</b>	<b>475K</b>
			<b>220K</b>

