



**PC**

*PHENIX FEE REVIEW* BNL - 11/21/96

# *Interpolating Pad Chambers*

- **Lund University**
  - Anders Oskarsson
  - Tom Svensson
  - Hans Ake Gustafsson
  - Sten Garpman
  - Lars Carlen
  - Ingvar Otterlund
  - Evert Stenlund
  - Kaj Soderstrom
  - Karim ElChenawi
- **McGill University**
  - Tommy Mark
  - Jean Barrette
  - Fuhu Liu
  - Paul McNeely
  - Jan Romanski
  - Nikolai Starinski
  - \* Ian Atatekin
  - Leo Nikkinen
  - Li Zhou
  - Dong Gan
  - Yujin Qi
  - Octavian Theoescu
- **Oak Ridge National Laboratory**
  - Bill Bryan
  - Usha Jagadish
  - Melissa Smith
  - Chuck Britton
  - Mike Simpson
  - Mark Allen
  - Lloyd Clonts
  - Gentry Jackson
  - \*Randall Smith

\* former participant



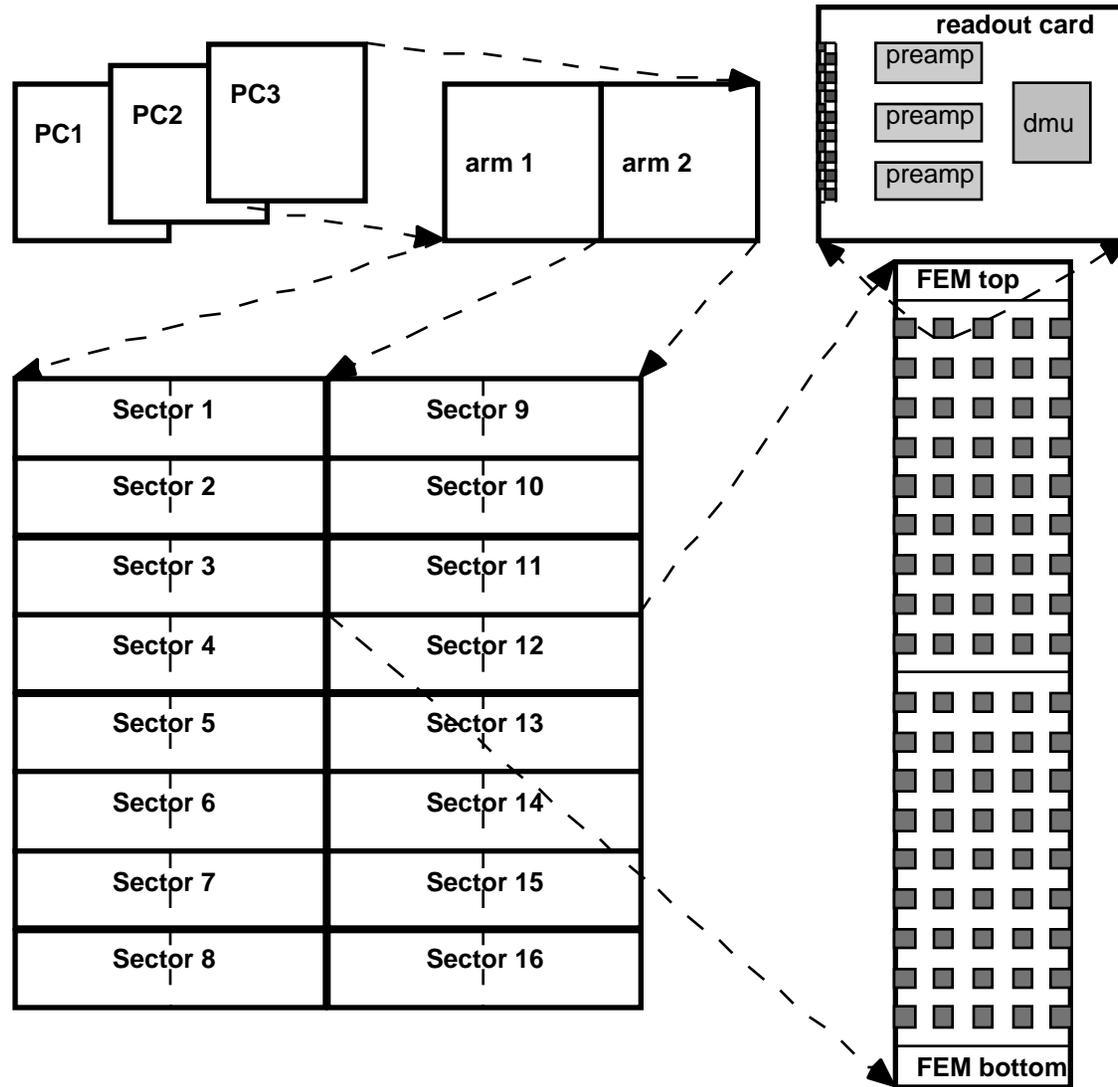
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*3D sketch of PC*



# PC

# breakdown diagram





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## *FEE components:*

- 3 16-sector interpolating Pad Chamber detectors
- 2 FEM's per sector(1 FEM for each half sector)
- 90 ReadOut Cards per sector(45 ROCs for each half sector)
- 1 DMU and 3 preamp chips per readout card
- PC1 + PC2 + PC3
  - 48(3x16) detector sector assemblies - McGill
  - 96(2x3x16) FEMs - ORNL
  - 4,320(90x3x16) ROCs - Lund
  - 4,320(90x3x16) DMU chips - Lund
  - 4,320(90x3x16) TGLD1 chips - ORNL
  - 4,320(90x3x16) TGLD2 chips - ORNL
  - 4,320(90x3x16) TGLD3 chips - ORNL
  - 207,360(16x3x90x3x16) channels



## PC

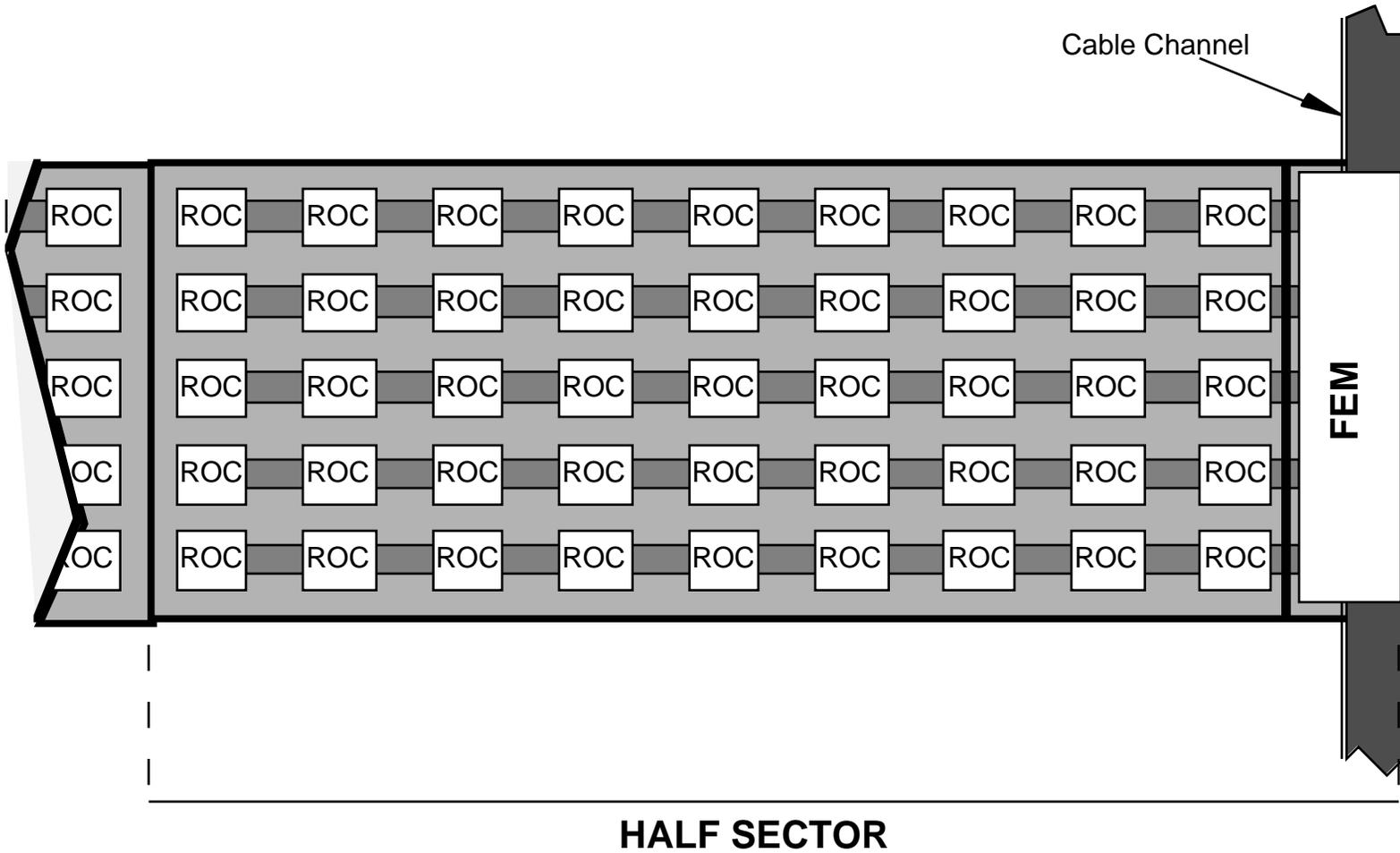
## *detector spec's*

	<u>PC1</u>	<u>PC2</u>	<u>PC3</u>
● detector capacitance:	5pF	16pF	20pF
● charge sensitivity/MIP:	18fC	29fC	36fC
● min. charge of interest:	0.9fC	1.45fC	1.8fC
● max. channel rate:	200 counts/second		



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# *half sector block diagram*



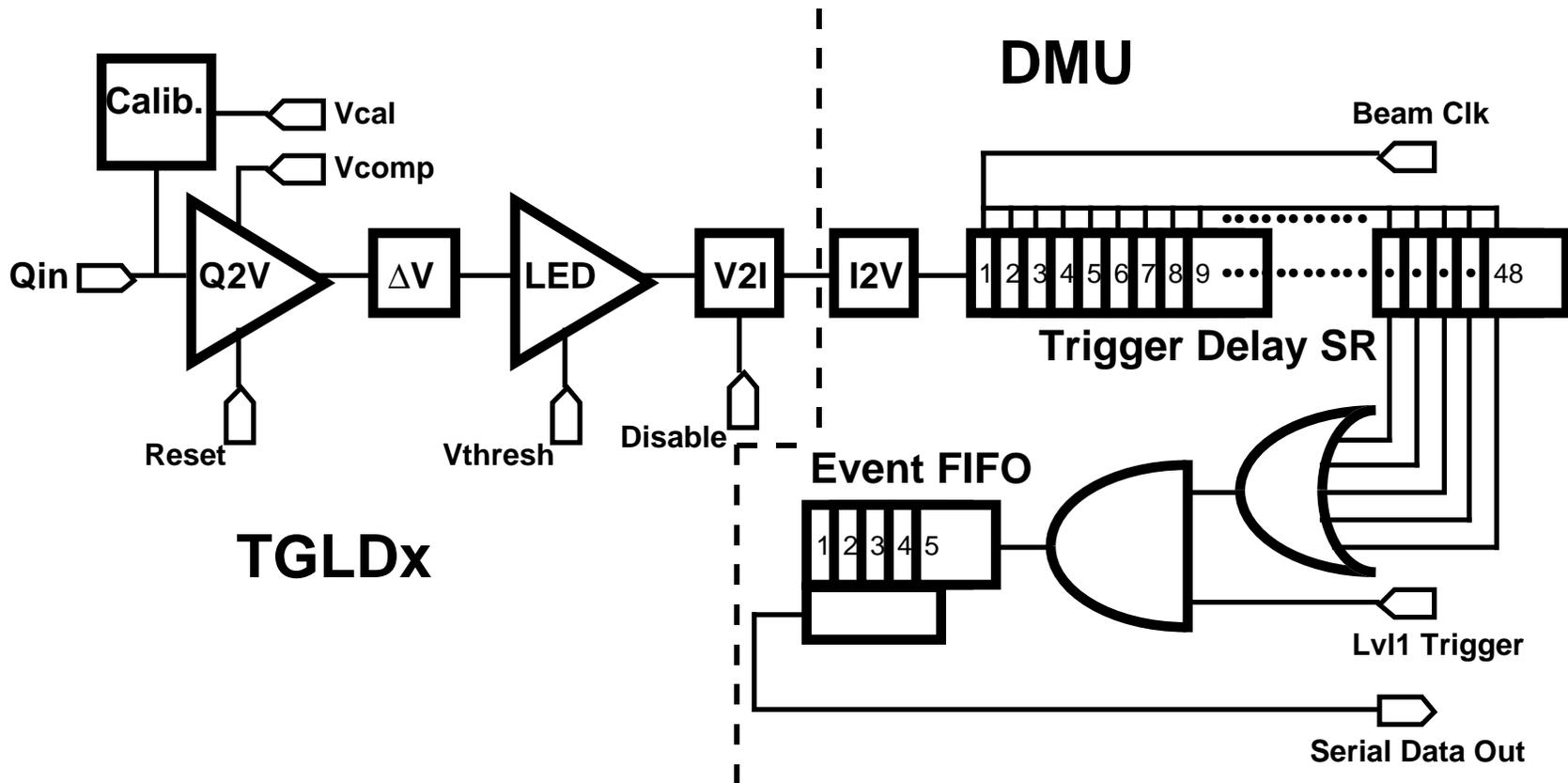


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*sector board & FEM layout*



# PC FEE channel block diagram





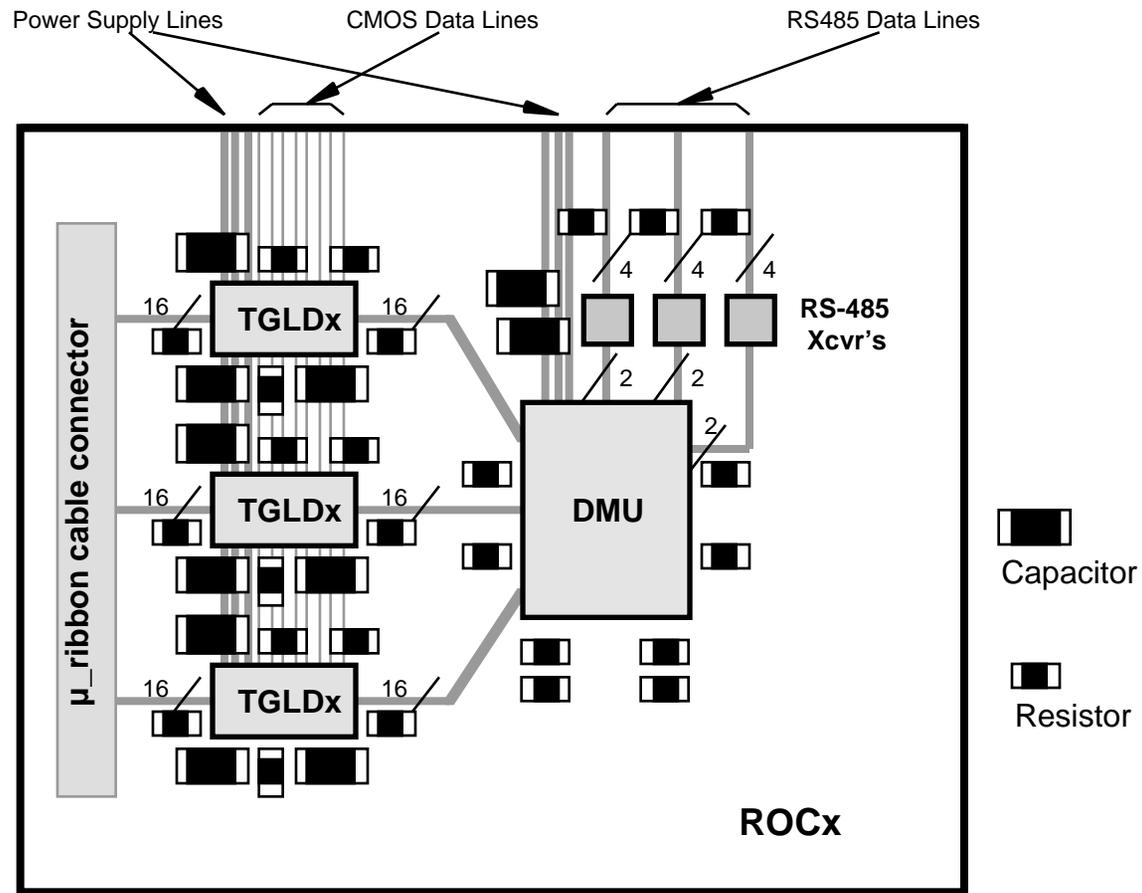
## **PC** *readout card construction*

- 45 48-channel readout cards per half sector
- 1 mm polyimide substrate
- chip on board construction
- 3 TGLD<sub>x</sub>, 1 DMU, low power RS-485  
drvr/rcvrs, chip resistors & capacitors
- solders to sector anode plane boards
- miniature ribbon connection to pixel plane



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# readout card block diagram





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*readout card layout*



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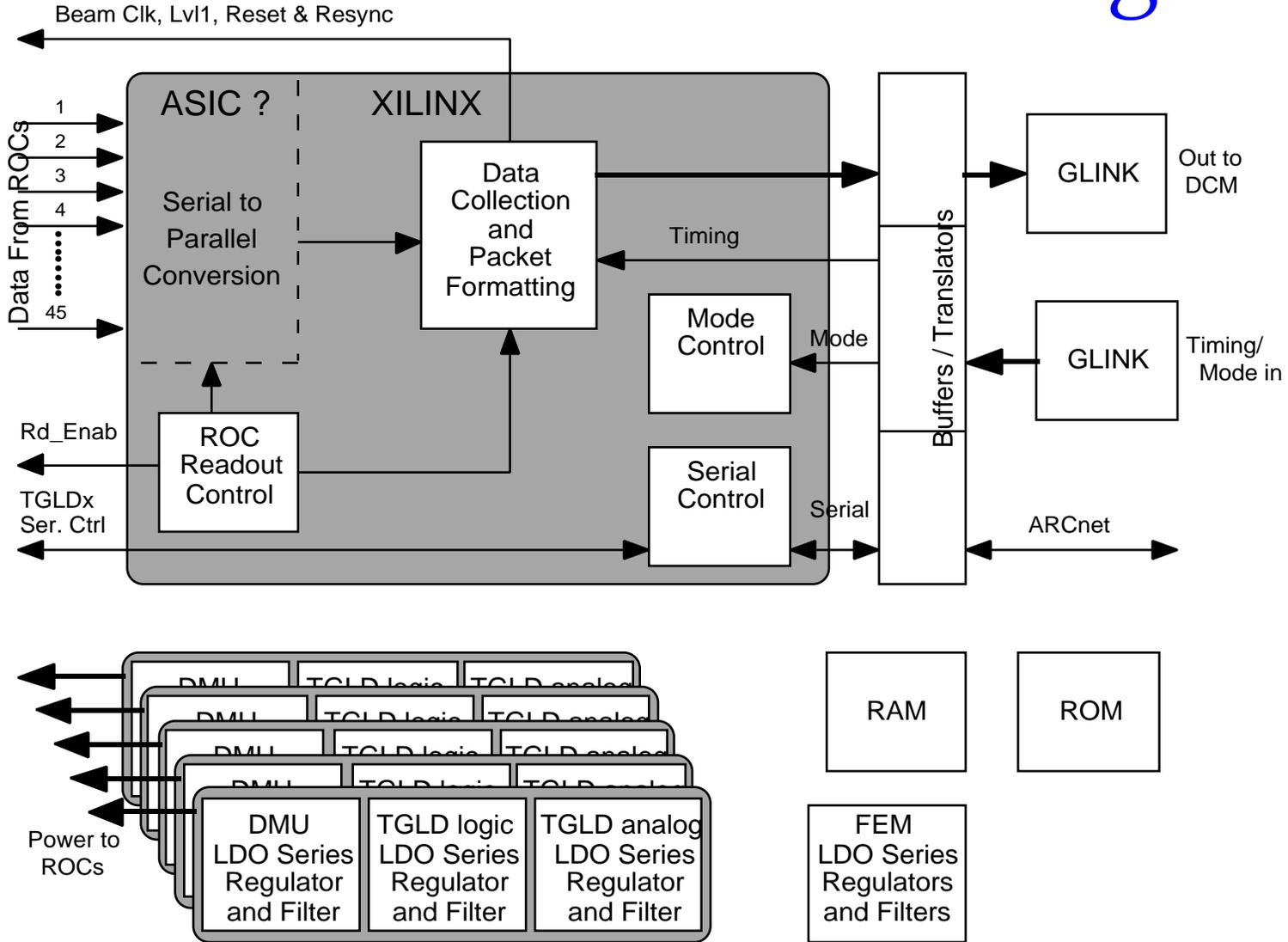
# *FEM card function*

- data mode:
  - fans out & xmits beam clock, level 1 trigger, reset & resync signals to ROCs
  - xfers event fifo contents from DMUs as required & verifies integrity via parity check
  - xforms 45 DMU serial streams to parallel stream for FEM data formatter
  - formats, tags and packetizes event data for xfer to DCM
- control & set-up mode:
  - xmits serial data to individual TGLDx chips for channel enable/disable, calibrate level , calibrate pulse & multiplex analog signal out address
  - reports mode and status information



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# FEM card block diagram

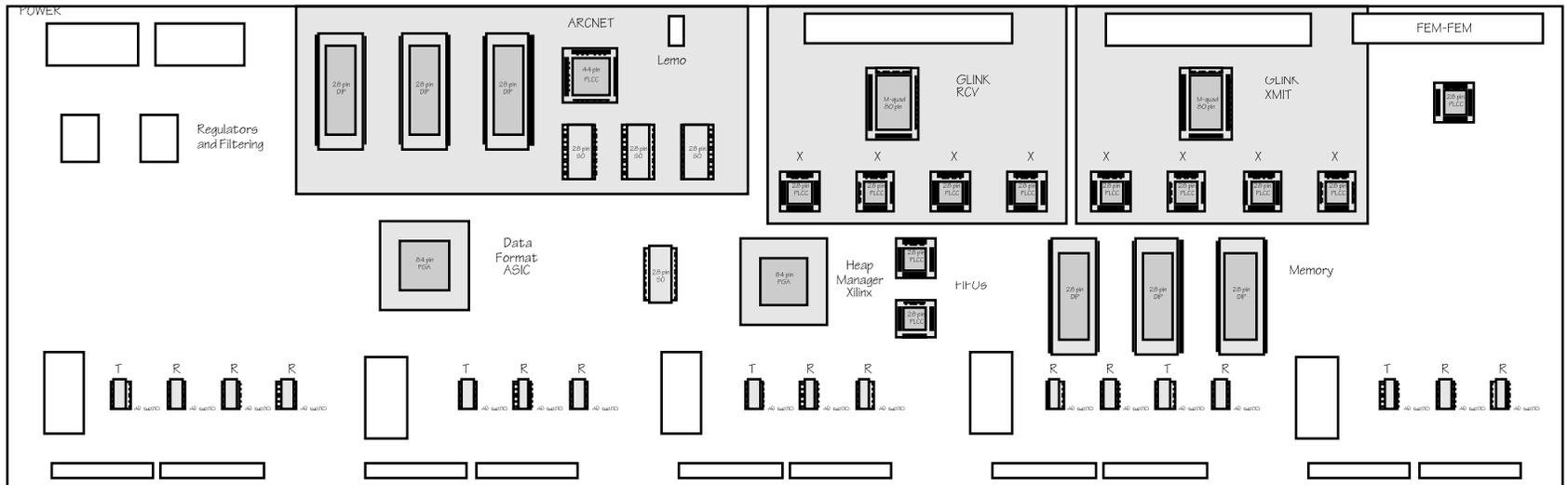






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# FEM board layout





## *PC power distribution and grounding*

- bias HV distributed via half sector detector anode planes
- low voltage power distributed via FEM board for each half sector
- separate digital and analog ground planes for FEM boards
- LDO series regulators used on FEM to isolate FEM's power from common voltage buses in detector
- 5 sets of 3 LDO series regulators regulate DMU +5, TGLDx +5 digital & TGLDx +5 analog for each row of 9 ROCs
- ROC power supplies are multiply bypassed
- local reference & bias voltages for TGLDx chips are multiply bypassed
- local pixel HV bias bypass caps are referenced back to the analog Vdd of the ROC



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*deliverables*

- **48(3x16) detector sector assemblies - McGill**
- **96(2x3x16) FEMs - ORNL**
- **4,320(90x3x16) ROCs - Lund**
- **4,320(90x3x16) DMU chips - Lund**
- **4,320(90x3x16) TGLD1 chips - ORNL**
- **4,320(90x3x16) TGLD2 chips - ORNL**
- **4,320(90x3x16) TGLD3 chips - ORNL**



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# *manufacturing plan*

- TGLDx chips: contract fab & test for known good die through Orbit or MOSIS; ship die to Lund or ROC assembler
- DMU chips: contract fab & test for known good die through AMS Europe; ship die to Lund or ROC assembler
- ORNL buys known good die RS-485 xcvr chips & ships die to Lund or ROC assembler
- ReadOut Card: contract assembly by Xicon Sweden; joint testing by Xicon & Lund; ship finished ROCs to McGill
- FEM boards: ORNL kits parts and contracts assembly of boards; ORNL tests assembled boards; ship finished FEMs to McGill
- Detector sector boards: contract fab of printed circuit boards for anode and pixel planes; McGill tests PCB planes, assembles & tests detector sectors with supplied ROCs and FEMs; ship finished sectors to BNL for installation



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# *readout card test plan*

- equivalent of FEM mock-up board will be provided to Lund from ORNL to exercise & accept/reject assembled ROCs
- Rejected ROCs with diagnosed bad/failed die will be reworked and recycled to above
- Mock-up FEM will calibrate ROC on-chip charge calibration circuits with calibrated external “known” charge
- use on-chip charge calibrator & off-chip charge pulsers to test TGLDx & DMU chips for proper calibration and data acquisition function and to diagnose bad/failed die for accept/rework/reject of ROCs
- accepted ROCs will be serialized and test records of on-chip charge calibration will be generated
- ancillary test equipment will include PCs, digital & analog i/o boards and lab power supplies.
- test SW will be developed in Labview



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## *FEM test plan*

- dedicated PCFEE FEM test station will be assembled for FEM acceptance testing
- test station will include fixtures or mock-ups for simulating functions of half sector detector array of ROCs, serial control link, data g-link, timing & mode g-link and DCM
- ancillary test equipment will include PCs, digital & analog i/o boards, lab power supplies, programmable word generators and pulsers.
- test SW will be developed in Labview



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# simple PERT chart

