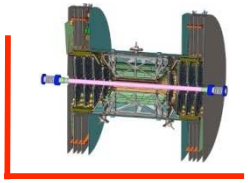
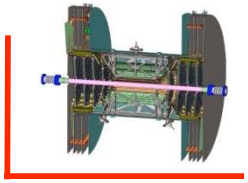


Sensors/FPHX Readout Chip

WBS 1.4.1/1.4.2

Jon S Kapustinsky

Design Decisions Leading to the FVTX Sensor Wedge and FPHX

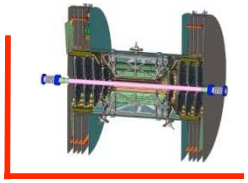


Technical risk minimization the key driver

- **Mini-strips maintain good resolution in r and phi with reasonable occupancy and manageable channel count**
- **Wire bonds replace initial idea to use bump bonds**
- **Chip placement moved from centerline of sensor to the edges**
  - **minimizes potential noise coupling between chip and sensor**
  - **facilitates implementation of decoupling between sensor bias and chip reference and avoids long path-length sensor return to ground**

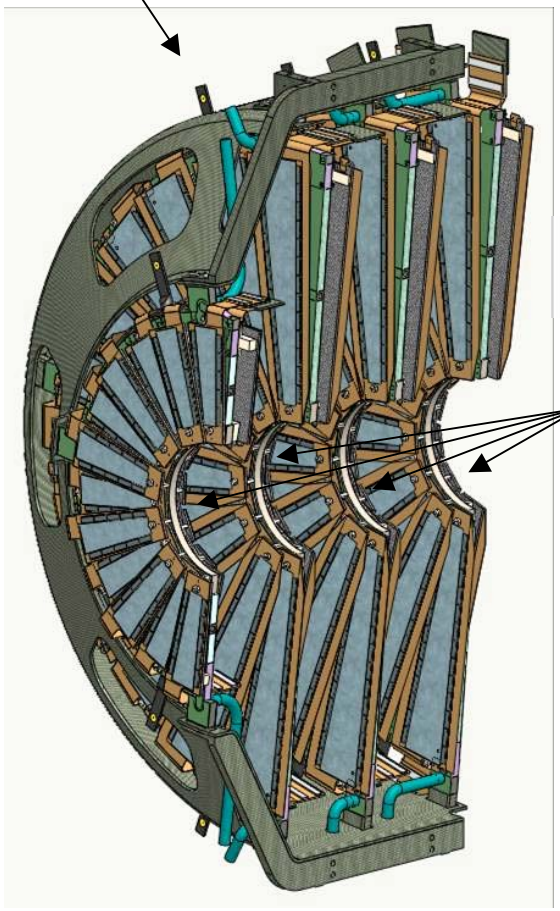
- **Wedge assembly unit based on ease of assembly**
- **HDI designed to match standard industry capability**
- **Readout architecture of the FPHX draws on previous successful designs; FPIX2, FSSR, and the SVX family of readout chips**
- **Low power design of the FPHX simplifies cooling and mechanics significantly**

FVTX Section View



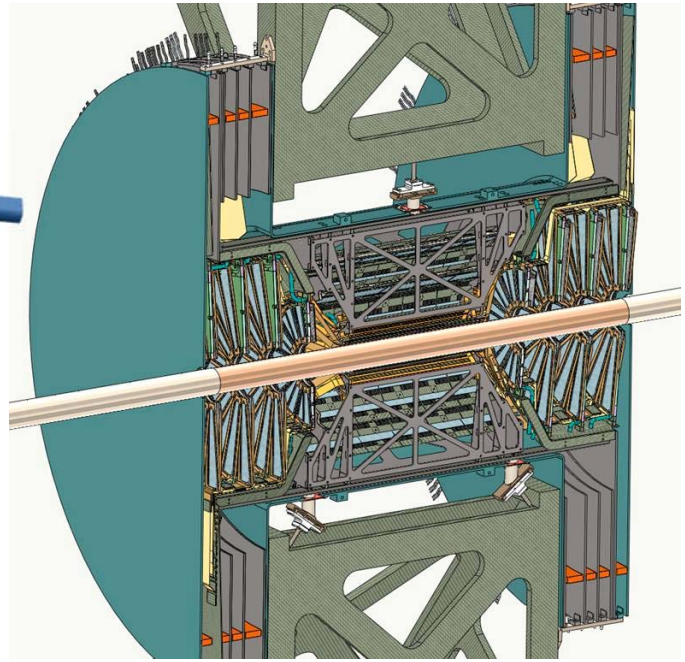
- Four disks on each side
- One small disk (~50mm) three large disks (~126mm)
- Mini-strips of 75 micron radial pitch: 3.45 -11.2 mm (large) and 3.45 – 6.55 mm (small)

½ of one endcap



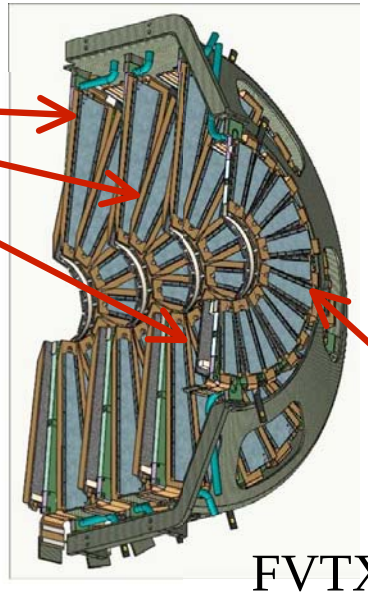
½ disks

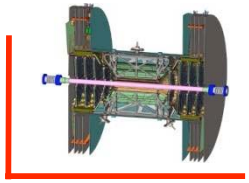
½ of the Barrel



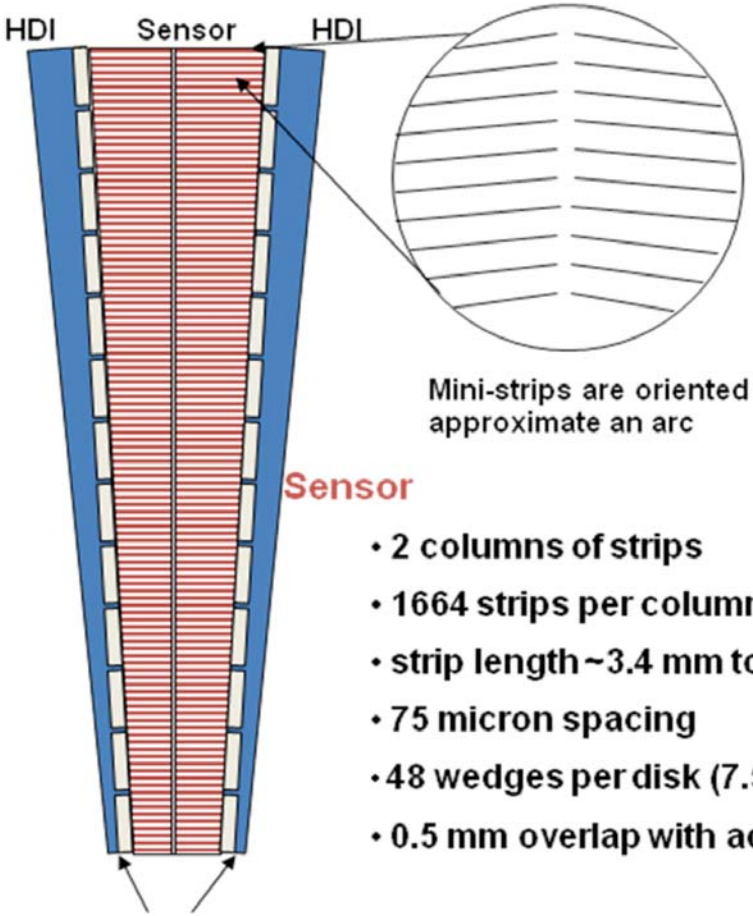
- Total strip count: 2 * 540,672 strips (zero suppressed)
- Total chip count: 2 * 4224 chips

FVTX Sensor Long Wedge



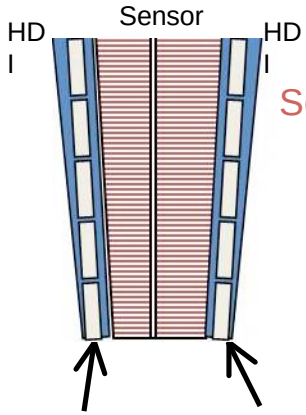


4 hermetic disks, z =18.5 to 38 cm



Overall length 126.8 mm
Overall width 8.8 mm i.r., 25.4 mm o.r.

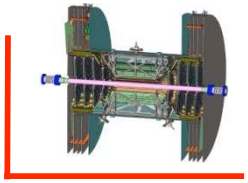
FVTX Sensor Short Wedge

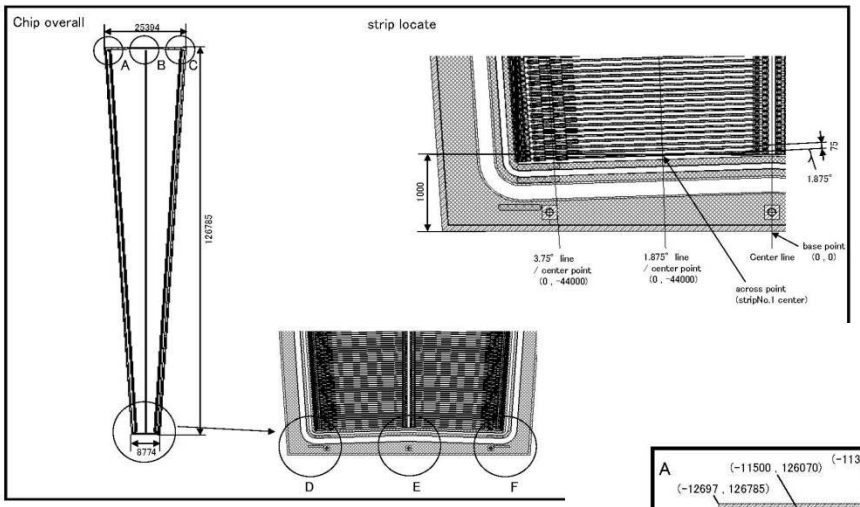


• 640 strips per column
• strip length
~ 3.4 mm to ~ 6.55mm

Overall length 50.1 mm
Overall width 8.8 mm i.r., 15.3 o.r

FVTX Sensors





UNM Probe station photo

p-implant on n-bulk
ac-coupled
1.5 MΩ polysilicon resistors
Depletion voltage < 100V
Resistivity 3 to 5 kΩ-cm

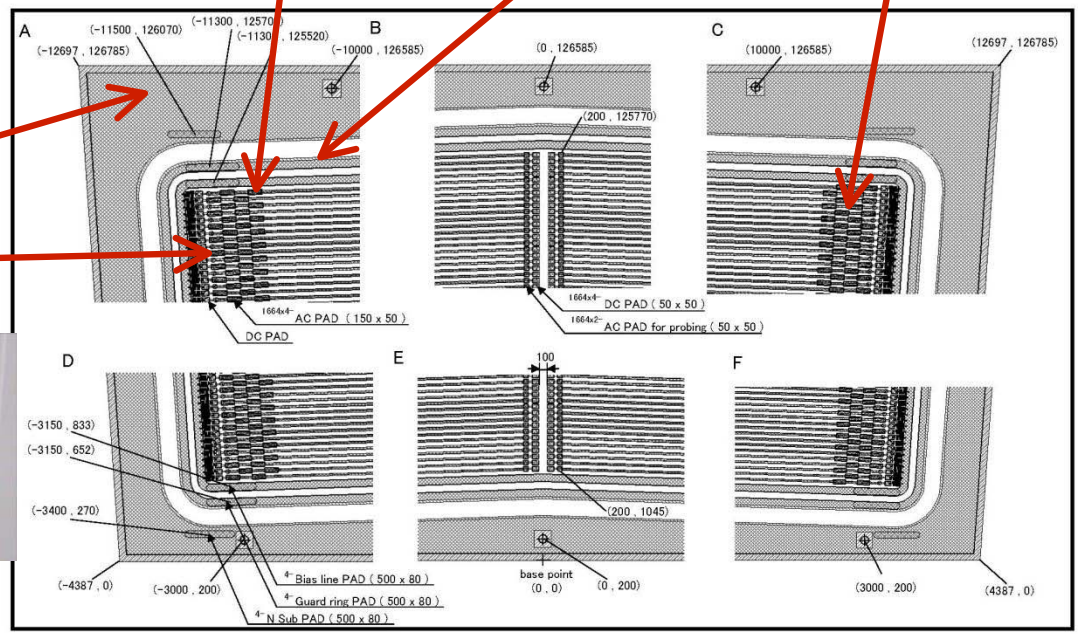
P-Bias Ring

Double Pad Rows

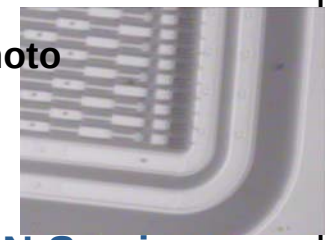
P-Guard Ring

N-Surround

Polysilicon Resistors



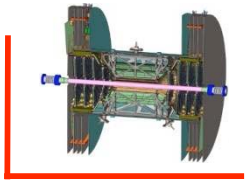
UNM Probe station photo



Initial Prototype, ON-Semi

Current Prototype, Hamamatsu – shipped 31 October, 2008

QA Silicon Sensor Wedges



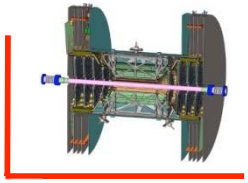
Complete QA specifications on file

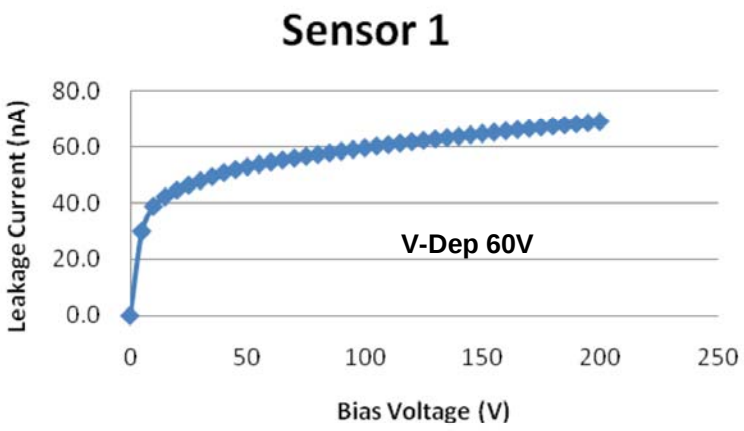
- Visual inspection to identify processing or handling flaws
- Current versus voltage characteristic curve for each sensor
- Capacitance versus voltage characteristic curve for each sensor
- Full depletion voltage and breakdown voltage for each sensor

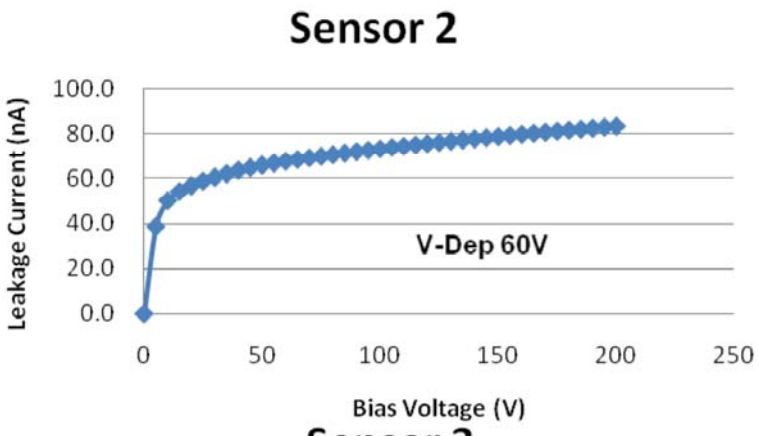
Sensors delivered from Hamamatsu are fully tested

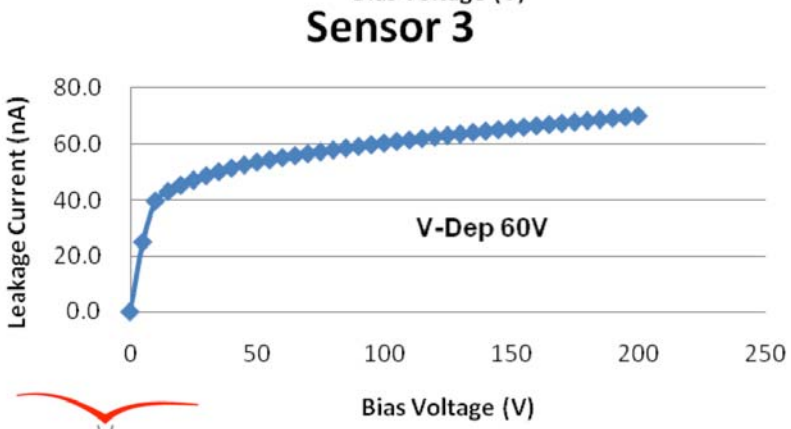
- Coupling capacitor integrity or short for each strip
- Implant open or short for each strip
- Polysilicon resistor open or short for each resistor

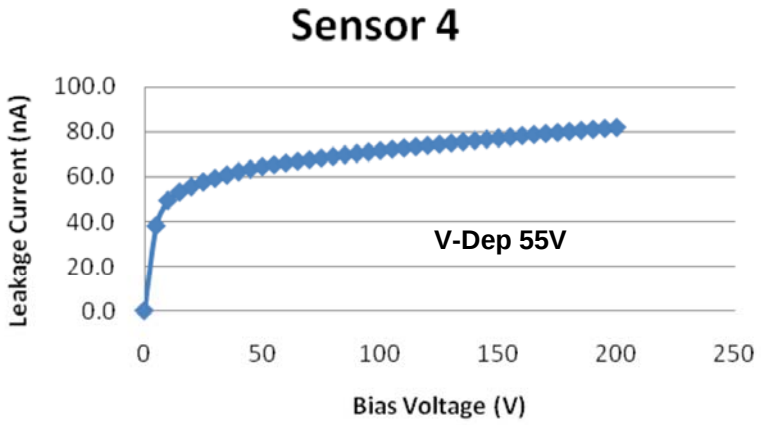
I/V Curves for Prototypes

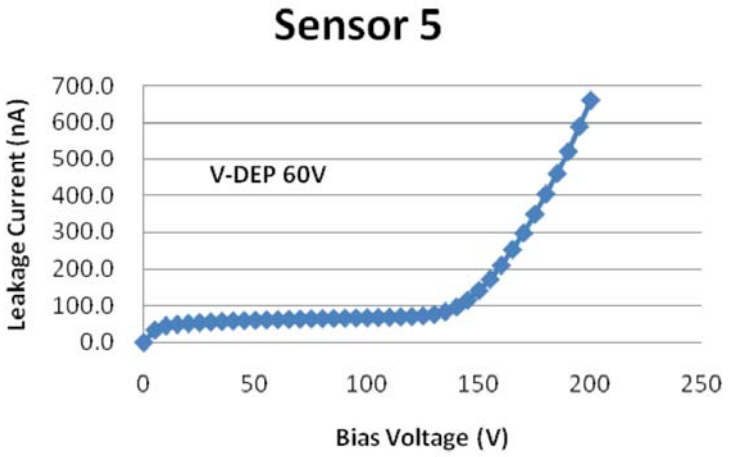






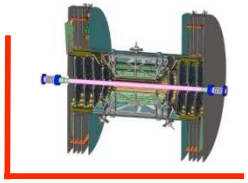






All strips on all 5 sensors are 100% good!

QA sensor manpower and facilities

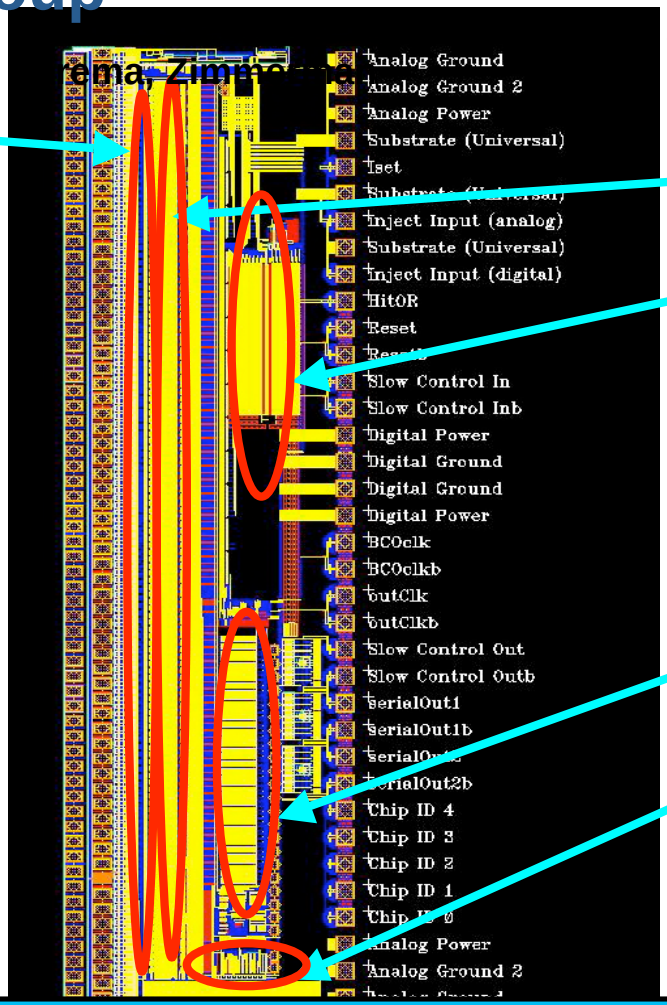


- 20 silicon sensors in a prototype run
- > 3 months in the schedule to QA prototypes
- Initial tests overseen by experts (Kapustinsky, Fields)
- 330 large, and 110 small silicon sensor wedges required for full FVTX, including spares (fully tested by Hamamatsu)
- Technician and student manpower QA over 5 months
- Test facilities exist at UNM, Prague

FPHX readout chip FNAL ASIC Group

Hoff, **ema, Zimmer**

Front End



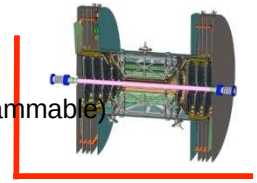
Chip size 2.7 x 9.1 mm

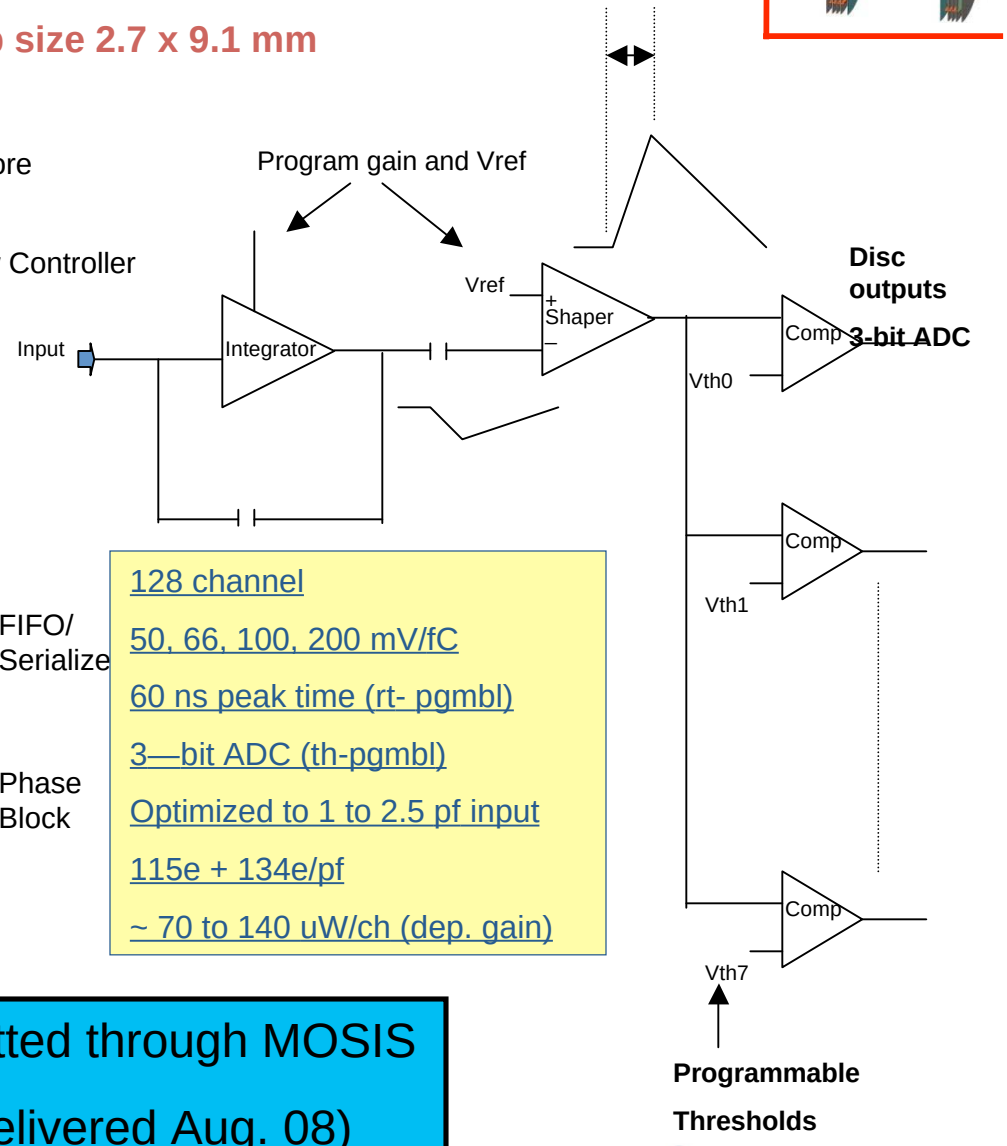
Core

Slow Controller

FIFO/ Serialize

Phase Block



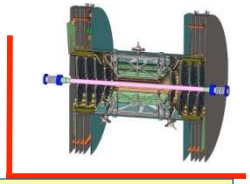


- 128 channel
- 50, 66, 100, 200 mV/fC
- 60 ns peak time (rt- pgmbl)
- 3—bit ADC (th-pgmbl)
- Optimized to 1 to 2.5 pf input
- 115e + 134e/pf
- ~ 70 to 140 uW/ch (dep. gain)

Fully functional chip design submitted through MOSIS

TSMC 0.25 micron process (delivered Aug. 08)

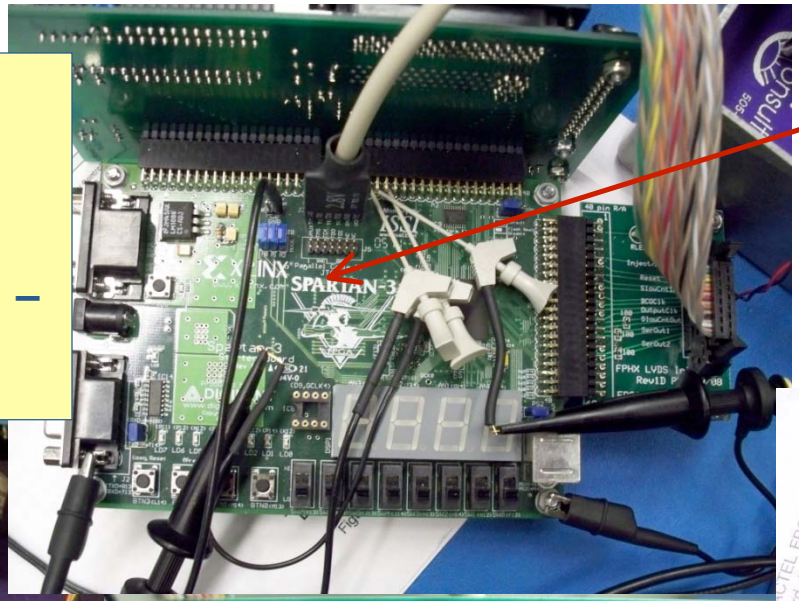
FPHX Test Stand at LANL



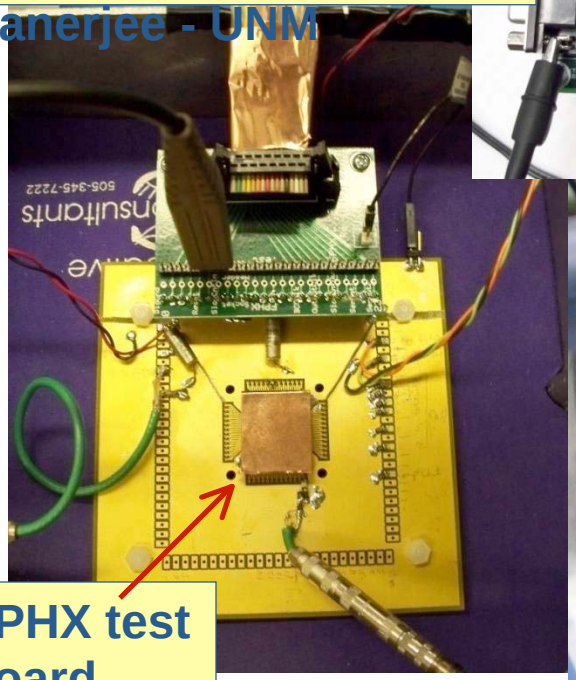
FPHX Test Stand

Brooks, Butsyk (PD), Kapustinsky, McGaughey, You (PD) – LANL

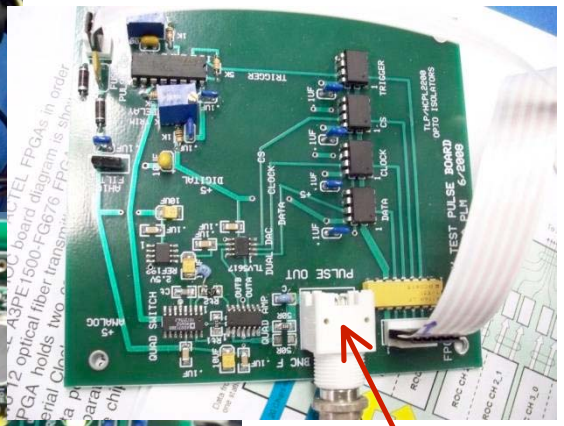
Banerjee - UNM

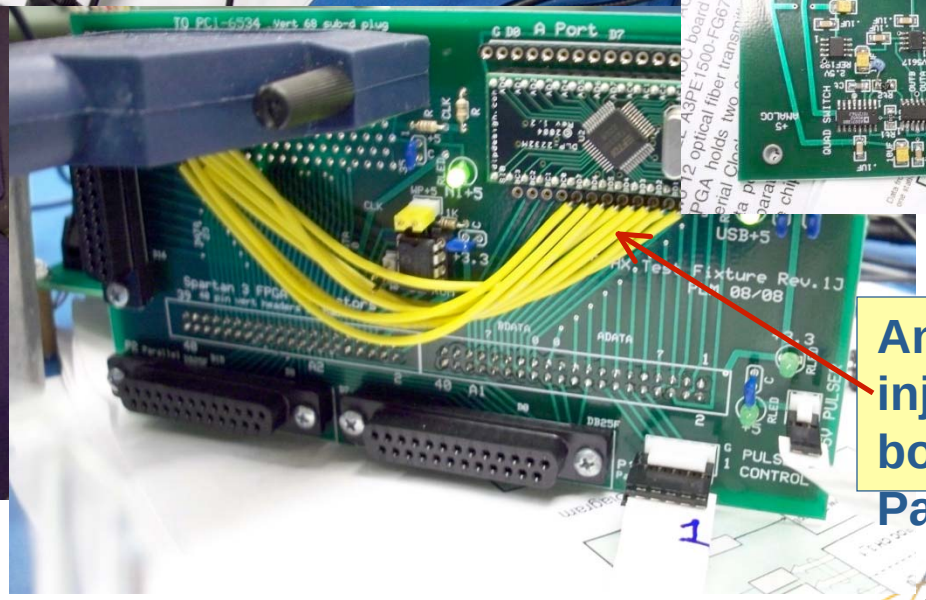


FPGA logic design and programming – Sergey Butsyk (LANL PD)



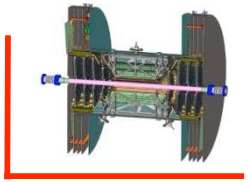
FPHX test board



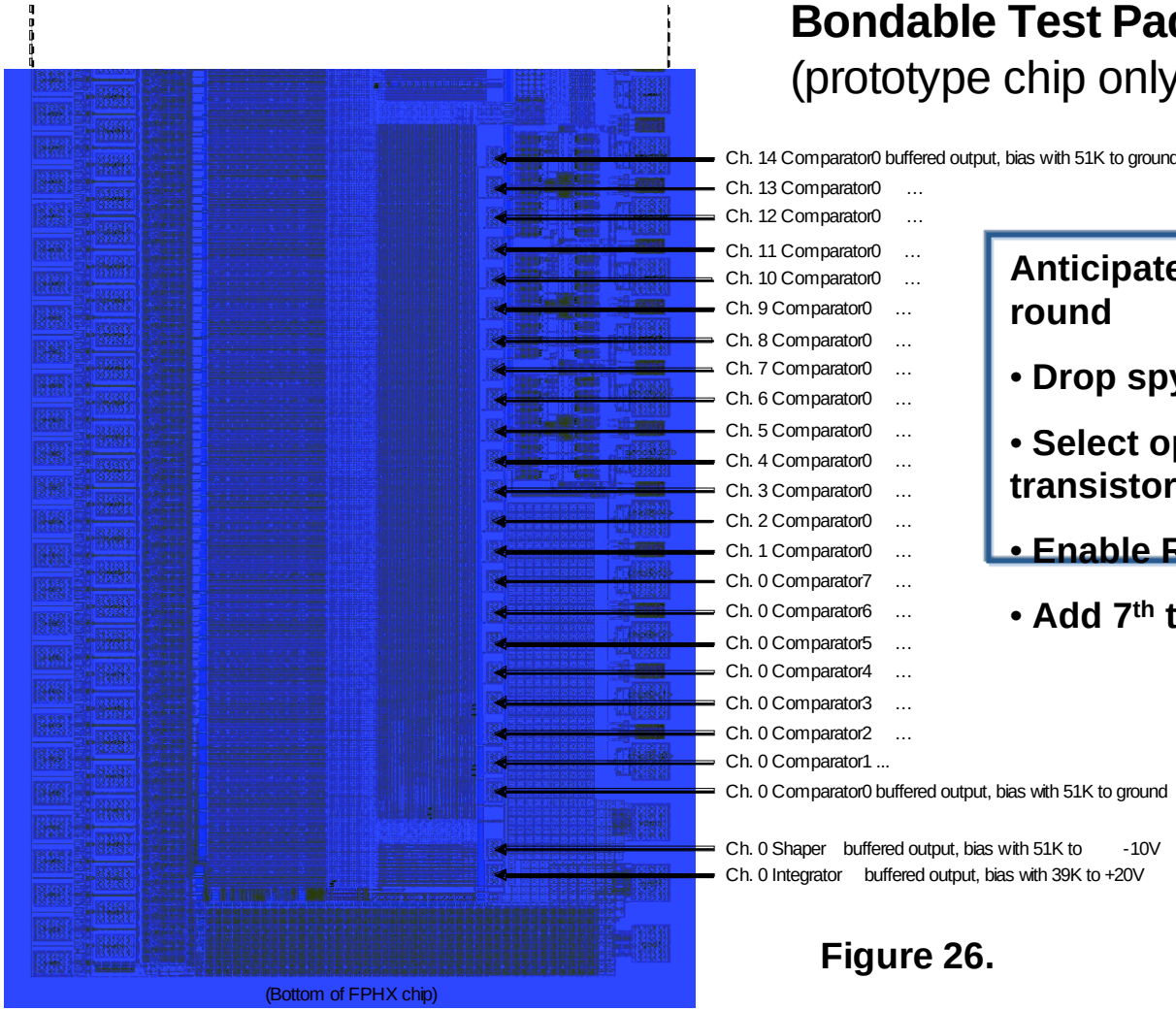


Analog pulse inject, interface boards

Pat McGaughey



Bondable Test Pads
(prototype chip only)



Anticipated changes in production round

- **Drop spy pads**
- **Select optimum W/L for input transistor**
- **Enable R/O on either serial line**
- **Add 7th time stamp bit**

Figure 26.

FPHX Preliminary Tests

Simulation results

With default parameters (N2Sel = 0100, Fb1Sel = 0100, GSel = 01, BWSel = 00100). Cin = 2 pF, Qin = 2000e.

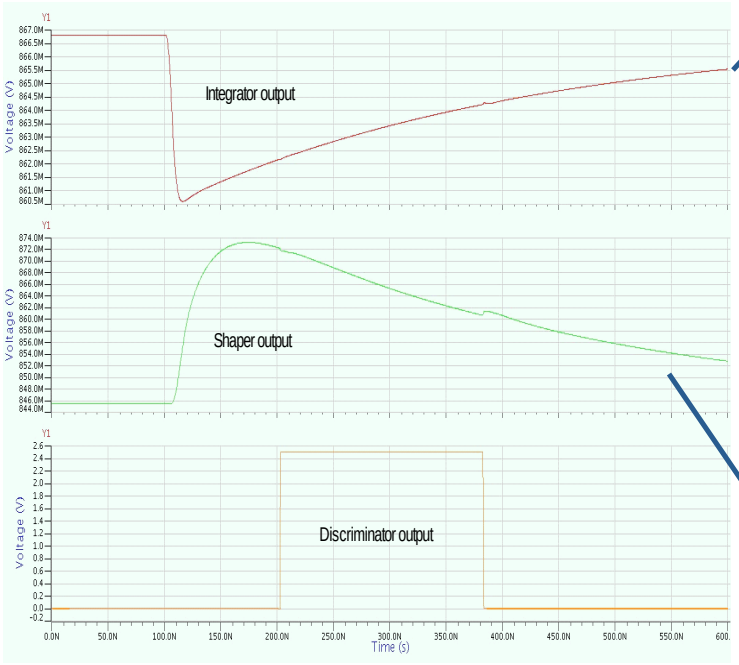
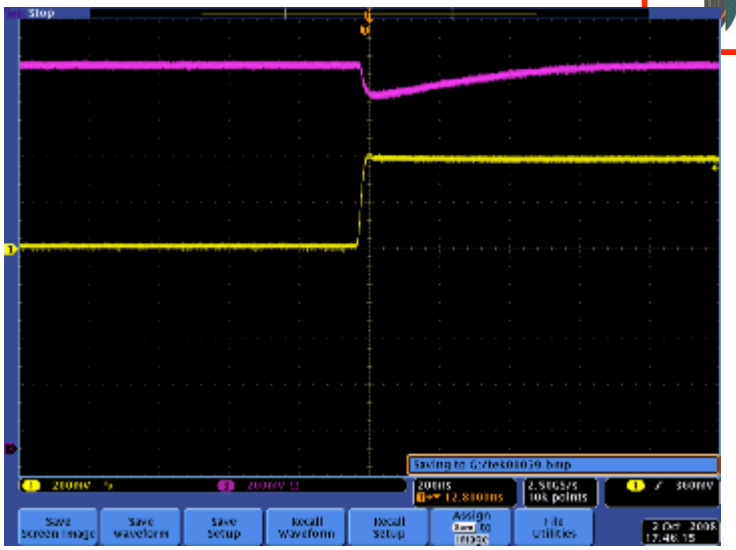
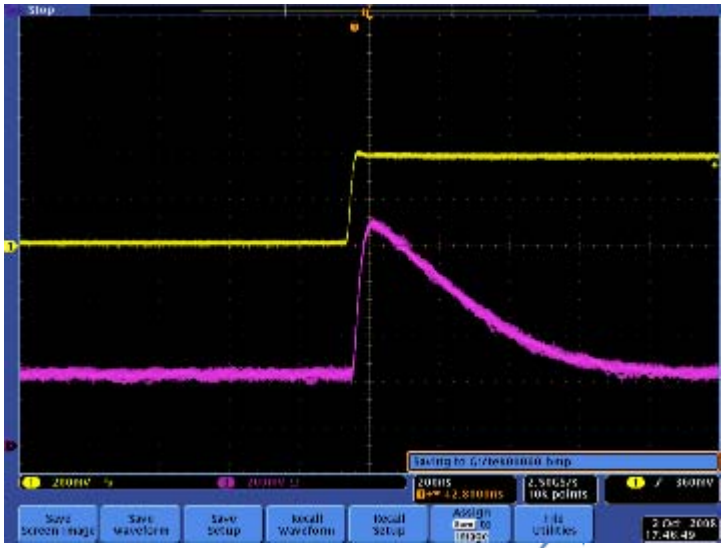


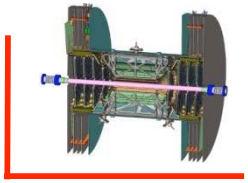
Figure 16.

Test Bench Data

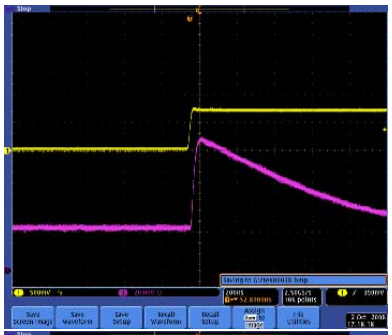




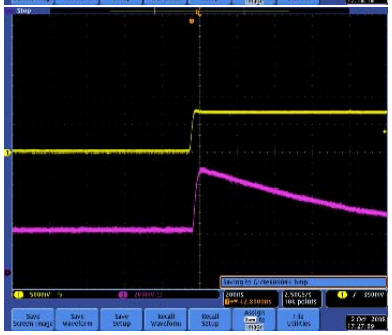
FPHX Programmable Bits



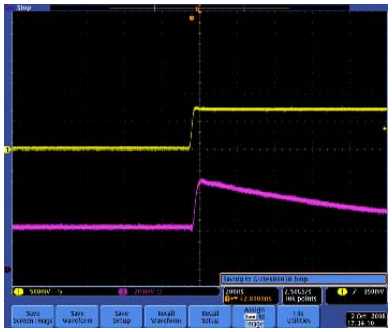
Gain



100 mV/fC

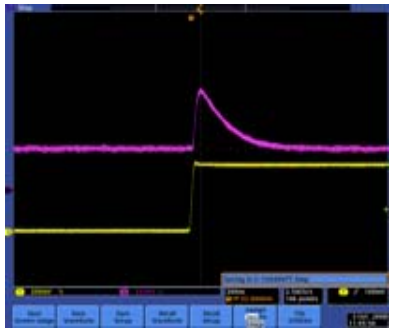


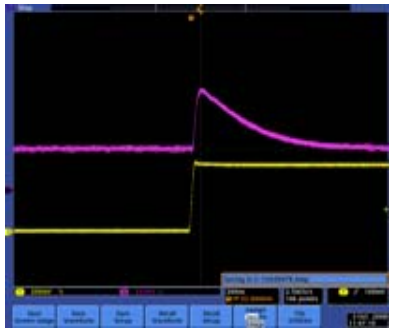
66 mV/fC

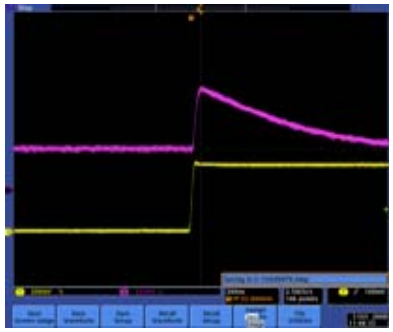


50mV/fC

Fall time



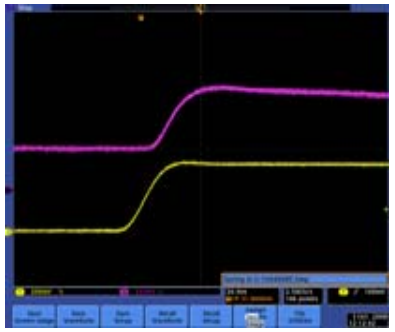


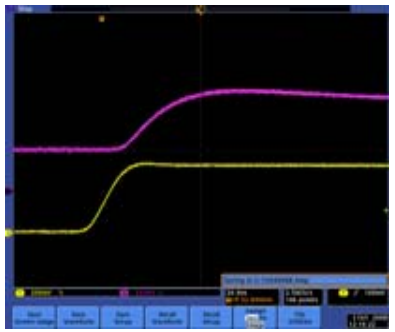


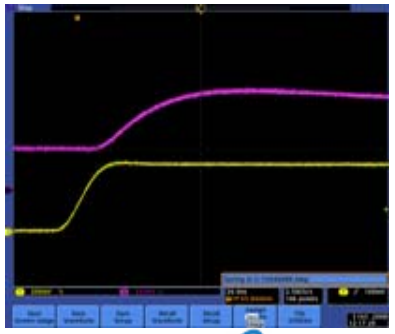
Fast
~250 ns

Slow
~2 µs

Rise time



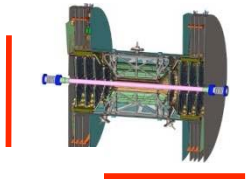




Fast
30 ns

Slow
90 ns

FPHX Chip back-end organization



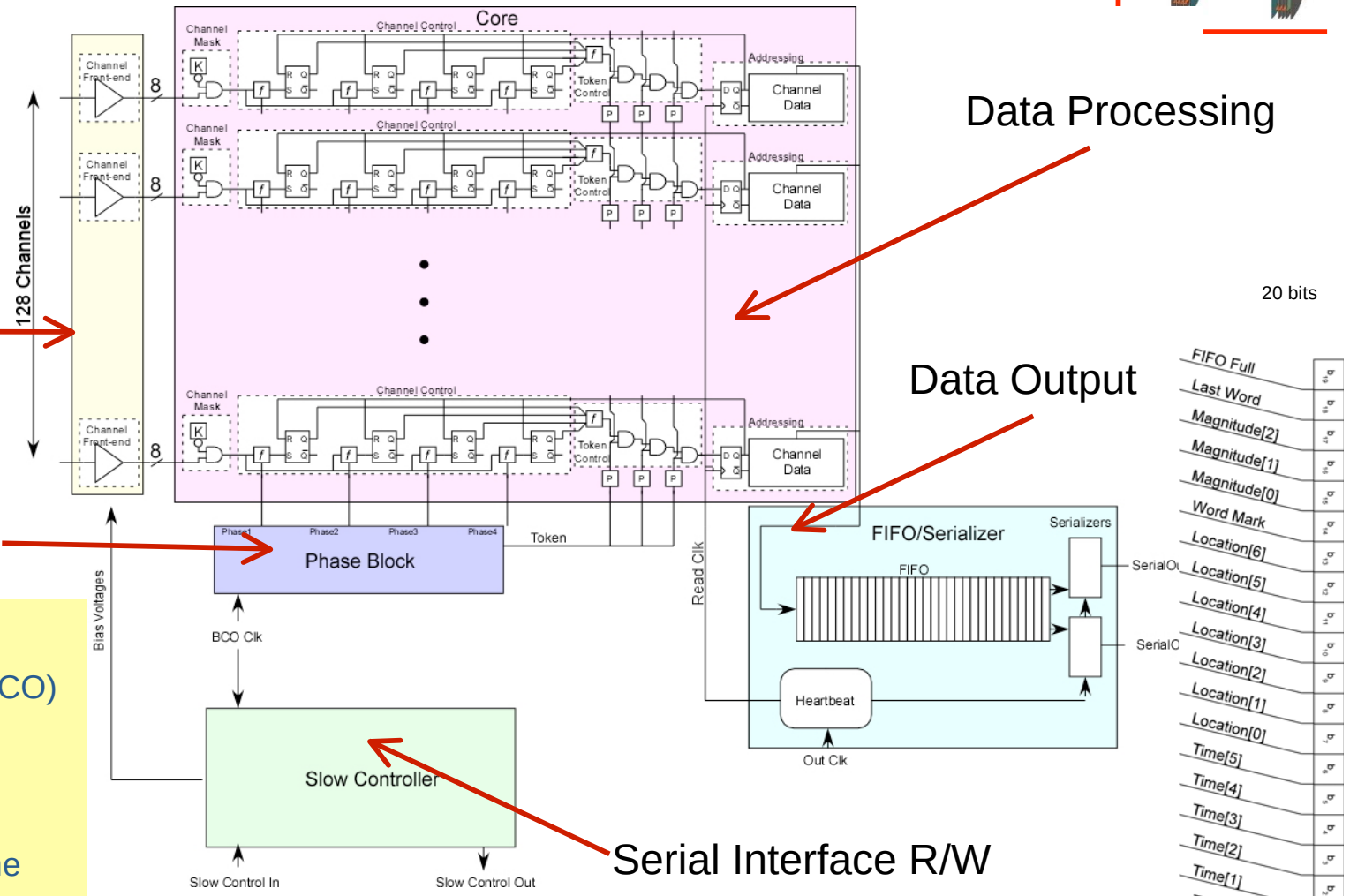
Data Processing

Analog

Data Output

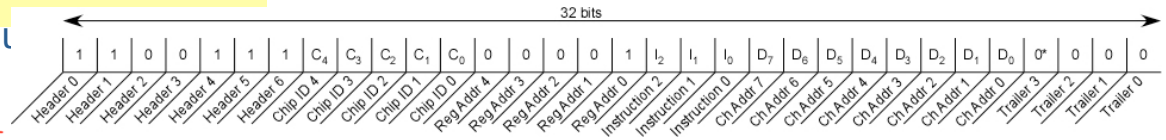
Phase Control

Serial Interface R/W

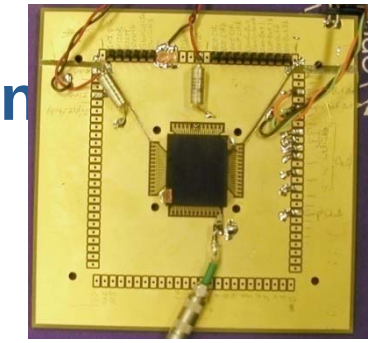


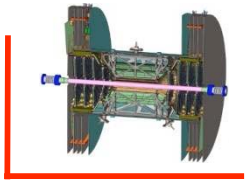
20 bits

- Data push architecture
- 10 MHz beam clock (BCO)
- 200 MHz data clock
- Zero suppressed
- Output 4 hits/chip in one BCO
- Approx. 300 u

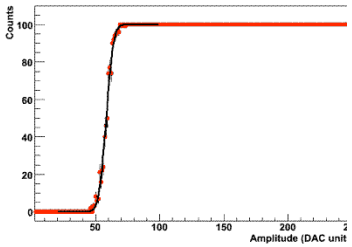


FVTX Technical Status - FPHX Testin

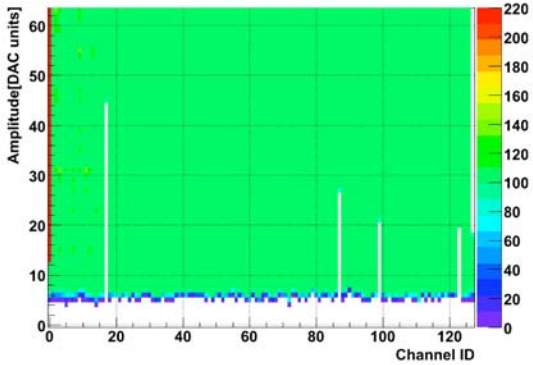


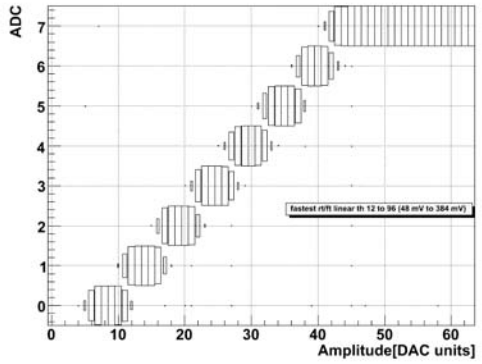


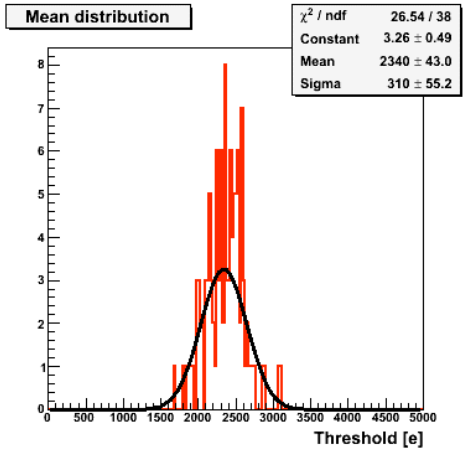
- ~200 electrons noise on most channels
- Threshold turn-on and distribution width as expected
- Programmable comparator thresholds work
- Known issues with 1st 15 channels because comparators are bonded out
- Overall performance is consistent with design specifications
- No issues uncovered s

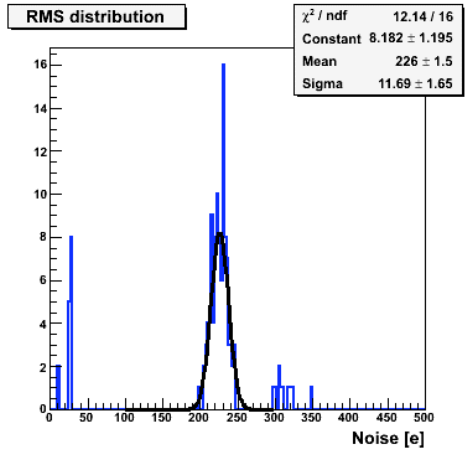


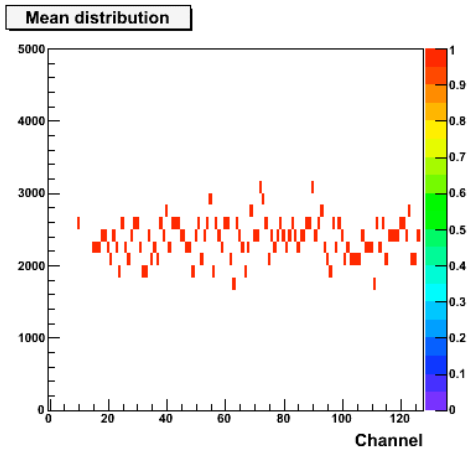
threshold turn-on curve

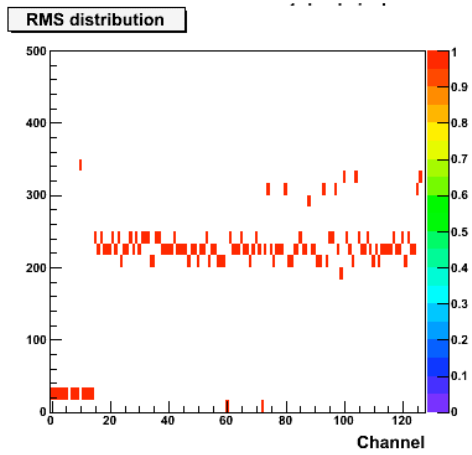




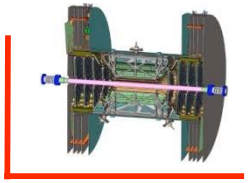






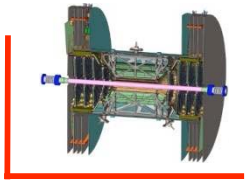


QA FPHX readout chip



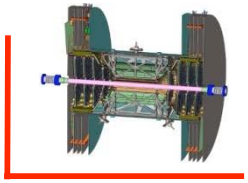
- Prototype bench tests at LANL and FNAL (Zimmerman and Hoff-FNAL, Kapustinsky, Brooks, McGaughey, Butsyk-LANL, Banerjee-UNM and Winter-Columbia)
- Bench tests analog and digital performance, setup parameter sensitivity, stability and system robustness
- System test with FPHX + HDI + Readout
- Probe station to test reference voltages and currents, noise and gain

QA FPHX manpower and facilities



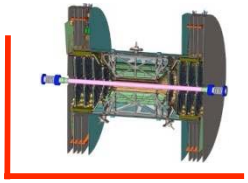
- Bench test stand facilities at FNAL, LANL, and soon UNM, and Columbia
- FNAL wafer probe station will be available for prototype and production testing
- Production will test 10-15 wafers, depending on yield (66% minimum assumption)
- Three months allotted for production wafer level tests, FNAL + students

Sensor design, production and testing

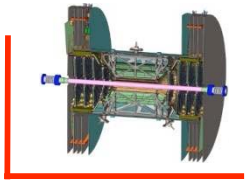


WBS	Item	Date
1.4.1.2.1	Design prototype sensor mask	07/08/08 done
1.4.1.2.2	Process prototype sensors	10/28/08 done
1.4.1.2.3	Test prototypes	02/10/09 finish
1.4.1.2.4	Wire-bond sensor to FPHX	12/17/08 start
1.4.1.3.1	Submit production sensors	02/11/09 start
1.4.1.3.2	QA production sensors	09/15/09 finish

FPHX design, production and testing

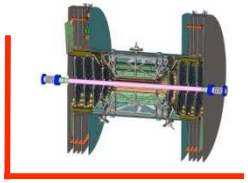


WBS	item	Date
1.4.2.3	FPHX layout design	04/10/08 done
1.4.2.6	Design review	04/14/08 done
1.4.2.4.1	Submission to MOSIS	08/22/08 done
1.4.2.4.2	Prototype tests	10/10/08 ongoing
1.4.2.4.3, 1.4.2.4.4	Submit second prototype run	03/25/09 start
1.4.2.4.5	Test second prototype	06/17/09 start
1.4.2.4.9	Second run performance	12/16/09
1.4.2.5.1	Submit engineering run (production run)	12/17/09 start
1.4.2.5.2	Test production wafers	04/01/10 start



Summary

- Sensor design, mask and prototype production complete
- Sensor QA ongoing for the next several months, incl. FPHX
- Production sensor order scheduled February 09
- FPHX first round fully functional prototype complete
- Bench tests validate analog and digital performance specs
- FPHX second round submission scheduled March 09
- FPHX production submission scheduled December 09

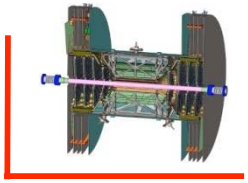


Backup Slides

PHENIX

Los Alamos NATIONAL LABORATORY

Hamamatsu Test Data



SerialNo. :	1
Vfd[V]:	60

VR/	Id[nA]	Ct[pA]
0	0.1	22013
5	30.0	3448
10	38.9	1853
15	42.3	1425
20	44.6	1202
25	46.5	1053
30	48.0	951
35	49.4	872
40	50.9	809
45	52.0	761
50	53.0	724
55	53.8	701
60	54.6	692
65	55.3	688
70	56.0	686
75	56.7	684
80	57.3	683
85	57.9	682
90	58.5	682
95	59.1	681
100	59.7	681
105	60.3	680
110	60.8	680
115	61.3	679
120	61.9	679
125	62.4	679
130	62.9	678
135	63.4	678
140	63.8	678
145	64.3	678
150	64.8	677
155	65.3	677
160	65.7	677
165	66.2	677
170	66.6	677
175	67.1	676
180	67.5	676
185	67.9	676
190	68.3	676
195	68.7	676
200	69.1	676

NG channels:
nothing

SerialNo. :	2
Vfd[V]:	60

VR/	Id[nA]	Ct[pA]
0	0.0	21715
5	38.5	3134
10	50.2	1843
15	54.2	1417
20	56.8	1195
25	58.9	1046
30	60.6	944
35	62.1	866
40	63.7	803
45	64.9	755
50	65.9	719
55	66.8	698
60	67.7	690
65	68.4	687
70	69.2	685
75	69.9	684
80	70.6	683
85	71.2	682
90	71.9	681
95	72.5	681
100	73.1	680
105	73.8	680
110	74.4	679
115	75.0	679
120	75.5	679
125	76.1	678
130	76.6	678
135	77.2	678
140	77.7	678
145	78.2	678
150	78.7	677
155	79.2	677
160	79.7	677
165	80.2	677
170	80.7	677
175	81.1	676
180	81.6	676
185	82.0	676
190	82.5	676
195	82.9	676
200	83.4	676

NG channels:
nothing

SerialNo. :	3
Vfd[V]:	60

VR/	Id[nA]	Ct[pA]
0	0.0	21811
5	25.1	3198
10	39.7	1825
15	43.1	1404
20	45.3	1183
25	47.1	1037
30	48.6	935
35	50.1	856
40	51.4	796
45	52.5	749
50	53.5	714
55	54.3	696
60	55.1	689
65	55.8	687
70	56.5	685
75	57.2	684
80	57.9	683
85	58.5	682
90	59.1	681
95	59.7	681
100	60.3	680
105	60.9	680
110	61.4	679
115	62.0	679
120	62.5	678
125	63.0	678
130	63.5	678
135	64.0	678
140	64.5	677
145	65.0	677
150	65.5	677
155	66.0	677
160	66.4	677
165	66.9	676
170	67.3	676
175	67.8	676
180	68.2	676
185	68.7	676
190	69.1	676
195	69.5	676
200	69.9	675

NG channels:
nothing

SerialNo. :	4
Vfd[V]:	55

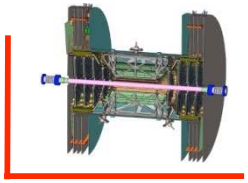
VR/	Id[nA]	Ct[pA]
0	0.0	21363
5	38.2	3001
10	49.5	1817
15	53.3	1399
20	55.7	1180
25	57.7	1033
30	59.3	932
35	60.9	854
40	62.3	793
45	63.5	747
50	64.5	713
55	65.4	696
60	66.2	689
65	67.0	687
70	67.7	685
75	68.5	684
80	69.1	683
85	69.8	682
90	70.5	681
95	71.1	681
100	71.7	680
105	72.4	680
110	73.0	680
115	73.5	679
120	74.1	679
125	74.7	678
130	75.2	678
135	75.8	678
140	76.3	678
145	76.8	677
150	77.4	677
155	77.9	677
160	78.4	677
165	78.9	677
170	79.4	676
175	79.8	676
180	80.3	676
185	80.8	676
190	81.3	676
195	81.7	676
200	82.1	676

NG channels:
nothing

SerialNo. :	5
Vfd[V]:	60

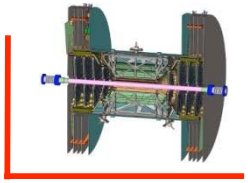
VR/	Id[nA]	Ct[pA]
0	0.0	21679
5	33.5	3052
10	45.6	1814
15	49.1	1396
20	51.5	1177
25	53.5	1031
30	55.1	931
35	56.6	853
40	58.1	792
45	59.2	746
50	60.1	712
55	61.0	694
60	61.7	688
65	62.5	685
70	63.2	683
75	63.9	682
80	64.6	681
85	65.2	680
90	65.8	680
95	66.5	679
100	67.1	679
105	67.8	678
110	68.4	678
115	69.2	678
120	70.4	677
125	72.3	677
130	76.2	677
135	83.8	676
140	95.8	676
145	115.0	676
150	140.9	676
155	171.3	675
160	209.2	675
165	252.2	675
170	297.1	675
175	348.5	675
180	403.5	675
185	458.8	675
190	521.6	674
195	589.3	674
200	660.6	674

NG channels:
nothing



FVTX Sensor Costs (AY$)

WBS	Item	Base	Actual cost	Quoted cost
1.4.1.2.1	Sensor mask set	$51.8k	$67.0k	
1.4.1.2.2	Sensor prototype	$25.9k	$36.9k	
1.4.1.2.3	Sensor production	$439.2k		$381.5k



FPHX Readout Chip Costs (AY$)

WBS	Item	Base	Actual	Quoted
1.4.2.1.2	1st FPHX proto run	$0	$175k	
1.4.2.4.4	2nd FPHX proto run	$194k		
1.4.2.5.1	Engineering FPHX run	$260k		