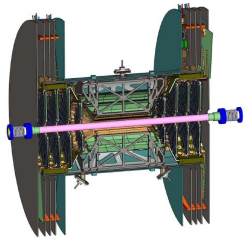


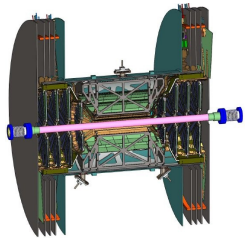
# Electrical Integration
# WBS 1.8.2

Eric J. Mannel
Columbia University
Electronics Project Engineer
VTX and FVTX

PHENIX

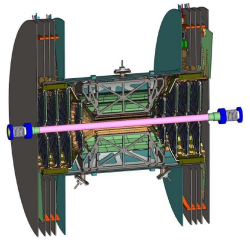
COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

# Electronics Integration



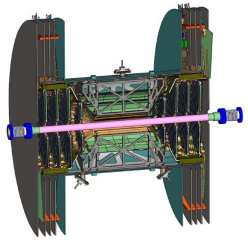
- Personnel
  - Eric J. Mannel: Electronics Project Engineer for both VTX and FVTX
  - Martin Purschke: PHENIX DAQ Coordinator
  - Steve Boose: DAQ Deputy Coordinator, Hardware
  - Ed Desmond: DAQ Deputy Coordinator, Software
  - FVTX Subsystem Managers and Electrical Engineers

# Project Engineer



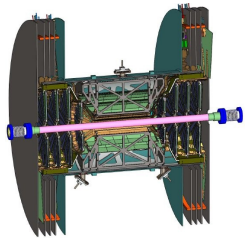
- Project Engineer's Responsibilities
  - Coordinate electronics production and electrical safety reviews.
  - Coordinate DAQ/Online integration.
  - Integrated Power/Grounding plan with VTX.
  - Approve with subsystem managers Q/A procedures and benchmarks.
  - Identify and ensure timely resolution of critical issues.
  - Work with subsystem managers to keep project on schedule and at cost.

# Electronics Review Process



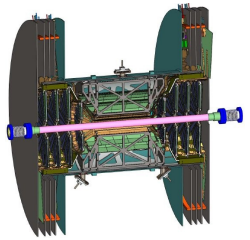
- Design Review Process:
  - Use Electronics Review Procedures similar to VTX project starting at the preproduction stage.
  - These procedures require:
    - Coordinate review with subsystem manager as design approaches completion.
    - Require all appropriate documentation to be posted for future reference (VTX/FVTX twiki):
      - Design files
      - Data sheets
      - Safety sheets
      - Q/A procedure documents

# Electronics Review Process



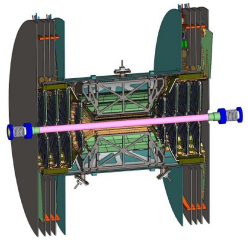
- Convene PHENIX internal review panel
- Review the module
  - Compatibility with PHENIX DAQ
  - Safety
  - Q/A
  - Performance
- Generate an “Action” list of issues that need to be followed up on prior to releasing the module for fabrication.
- Verify that all technical questions are properly addressed.
- Convene follow up session of review panel if necessary.
- Release module for fabrication.

# Electronics Review Process



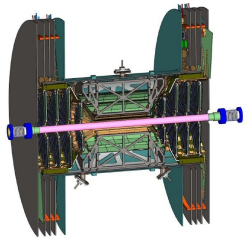
- Electrical Safety Reviews:
  - Held concurrent with the final production design review.
  - Contact PHENIX safety officer to request a safety review of production modules.
  - Work with subsystem manager to assemble all required safety documentation.
  - Meet with safety team and design team to address and resolve all safety questions.

# Electronics Review Process



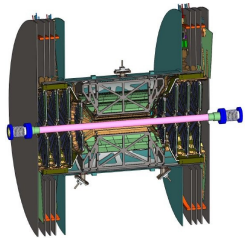
- Reviews held to date:
  - FPHX Design review.
  - Reviews held in February, March, and April 2008.
  - Included the chip designers, FVTX electronics designers and PHENIX DAQ experts.
  - Conclusion of the review process was to submit the chip in June 2008.
  - Early tests results show that the chip is functional and meets design specifications.

# Electronics Review Process



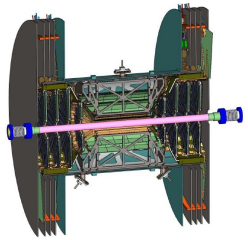
- FVTX Overall Electronics Design Review
  - Held in August 2008 to review the overall design of the FVTX electronics chain.
  - Cheng-Yi Chi, John Haggerty and Chuck Pancake were the reviewers.
  - Summary report with suggestions and concerns was submitted to the FVTX group in August 2008.

# Design and Safety Review Schedule - Tentative



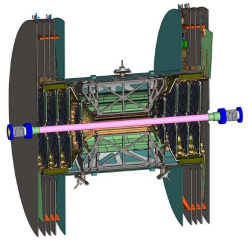
| Module | Preproduction Design Review | Production Design |
|---|---|---|
| Sensor | Complete | Feb 2009 |
| FPHX | Mar 2009 | Dec 2009 |
| HDI | Feb 2009 | July 2009 |
| ROC | Feb 2009 | July 2009 |
| FEM | Feb 2009 | July 2009 |
| Electrical Safety | | Dec 2009 |

# Electronics DAQ Integration



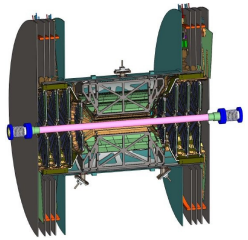
- PHENIX DAQ/ONCS Integration
  - Coordinate meetings with PHENIX DAQ and ONCS groups.
  - Assist with providing interface specifications.
  - Work with design teams to make sure that all interfaces are compatible with PHENIX DAQ and online systems.
  - Had initial meeting in January 2008 to review the general concept.
  - Follow up discussion planned for January 2009.

# Power and Ground



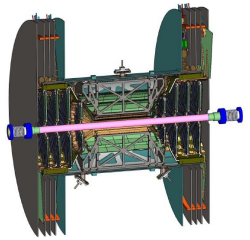
- Power and Ground Plan
  - Common plan for VTX and FVTX
    - VTX and FVTX isolated from each other and other PHENIX systems.
    - Shield around beam pipe and enclosure.
    - Star ground plan.
      - Single point connection to PHENIX clean ground
      - Flexibility in location of ground connections
    - Optical connections to Rack Room/DAQ.
    - Floating power supplies.

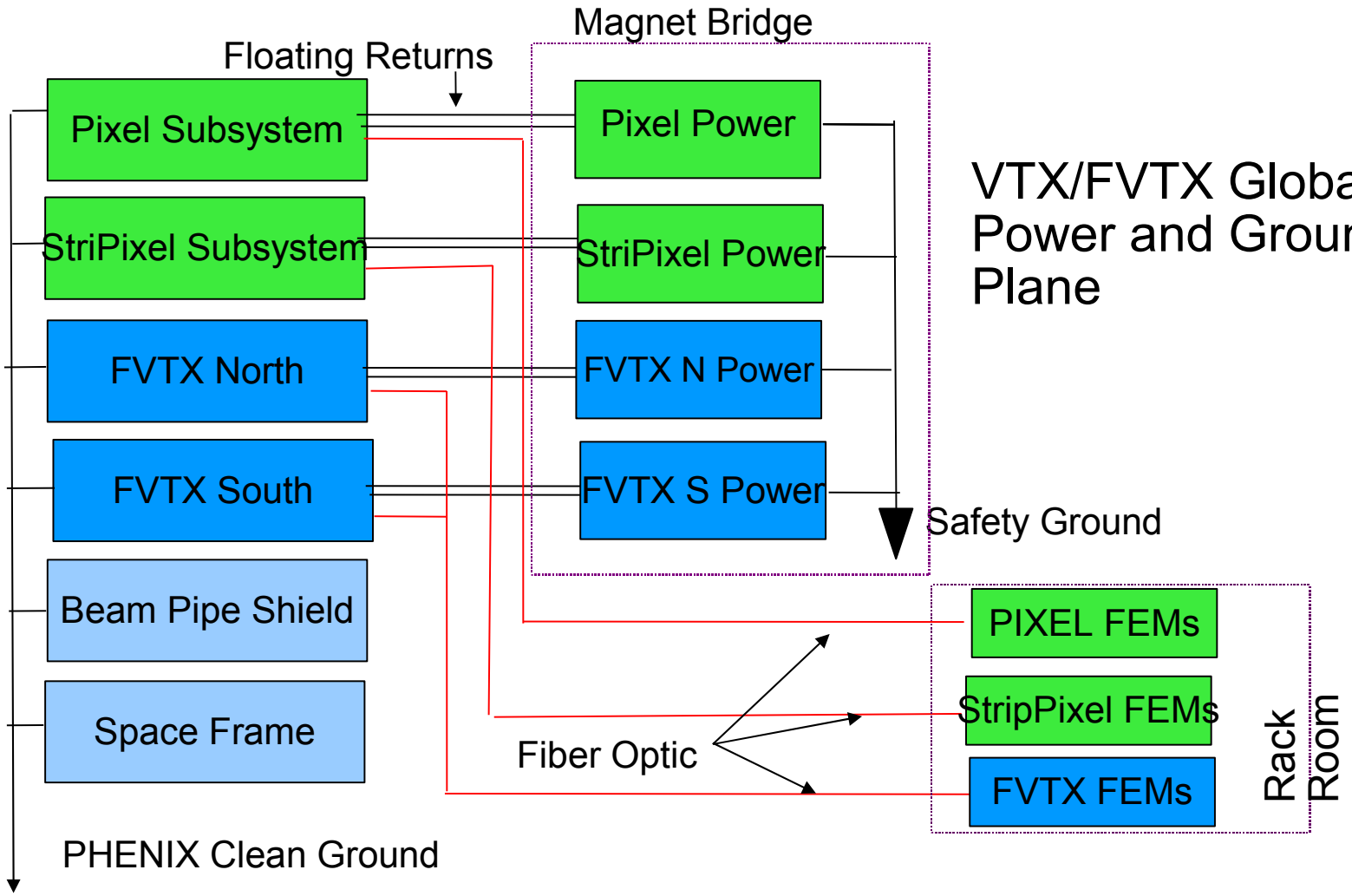
# Power and Ground



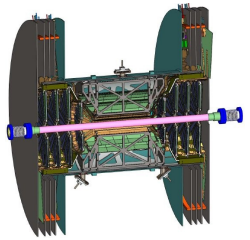
- When possible use same vendor for components
  - Wiener/ISEG for Bias
    - Evaluation model tested
      - » Mar-May 2008 (Used for VTX Pixel bias test)
      - » July-Sept 2008 (Software integration testing)
    - DAQ/ONCS group concludes that it will be easy to integrate into PHENIX
  - PHENIX standard low voltage power systems.

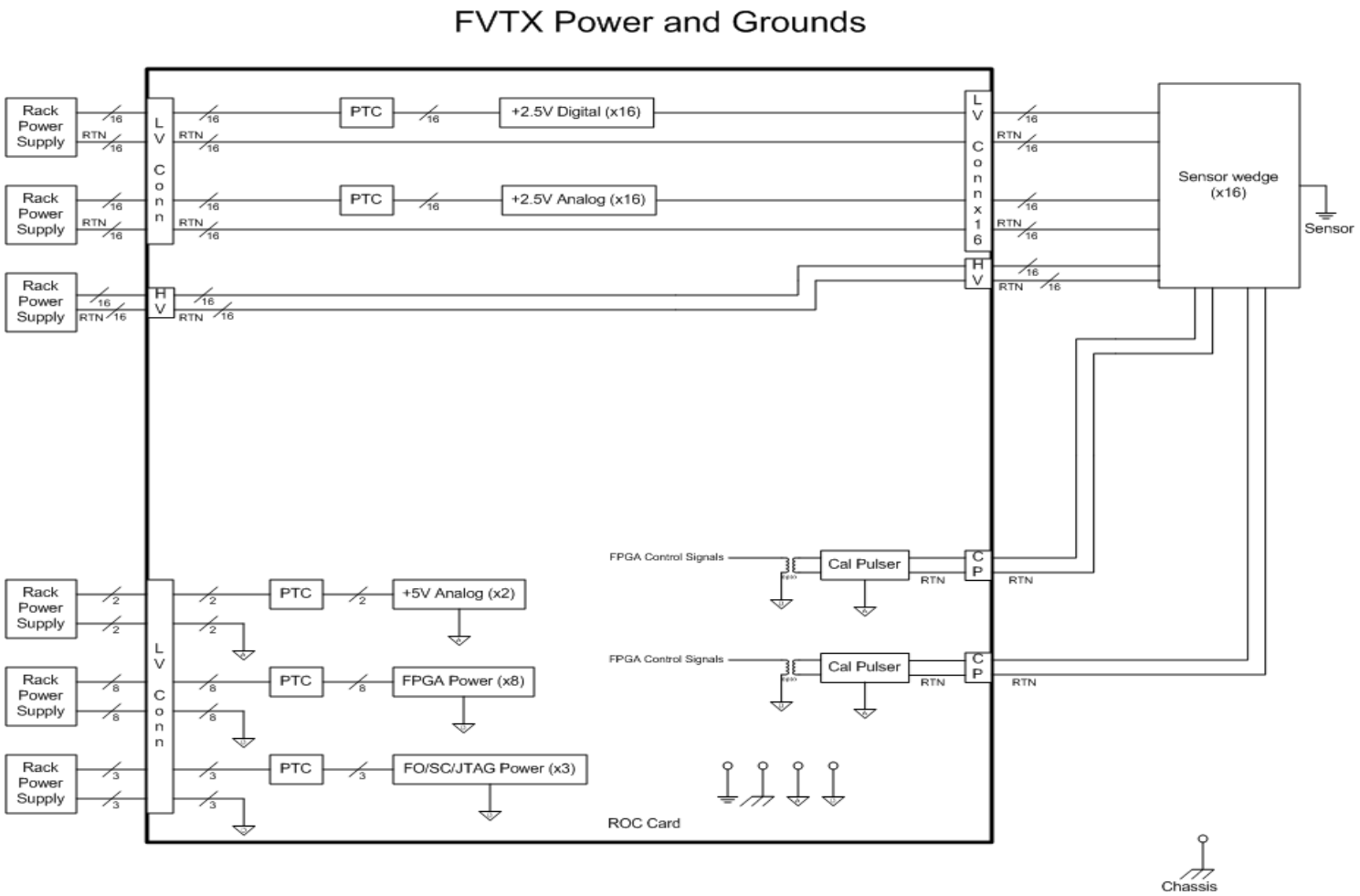
# Power and Ground



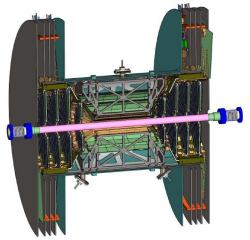


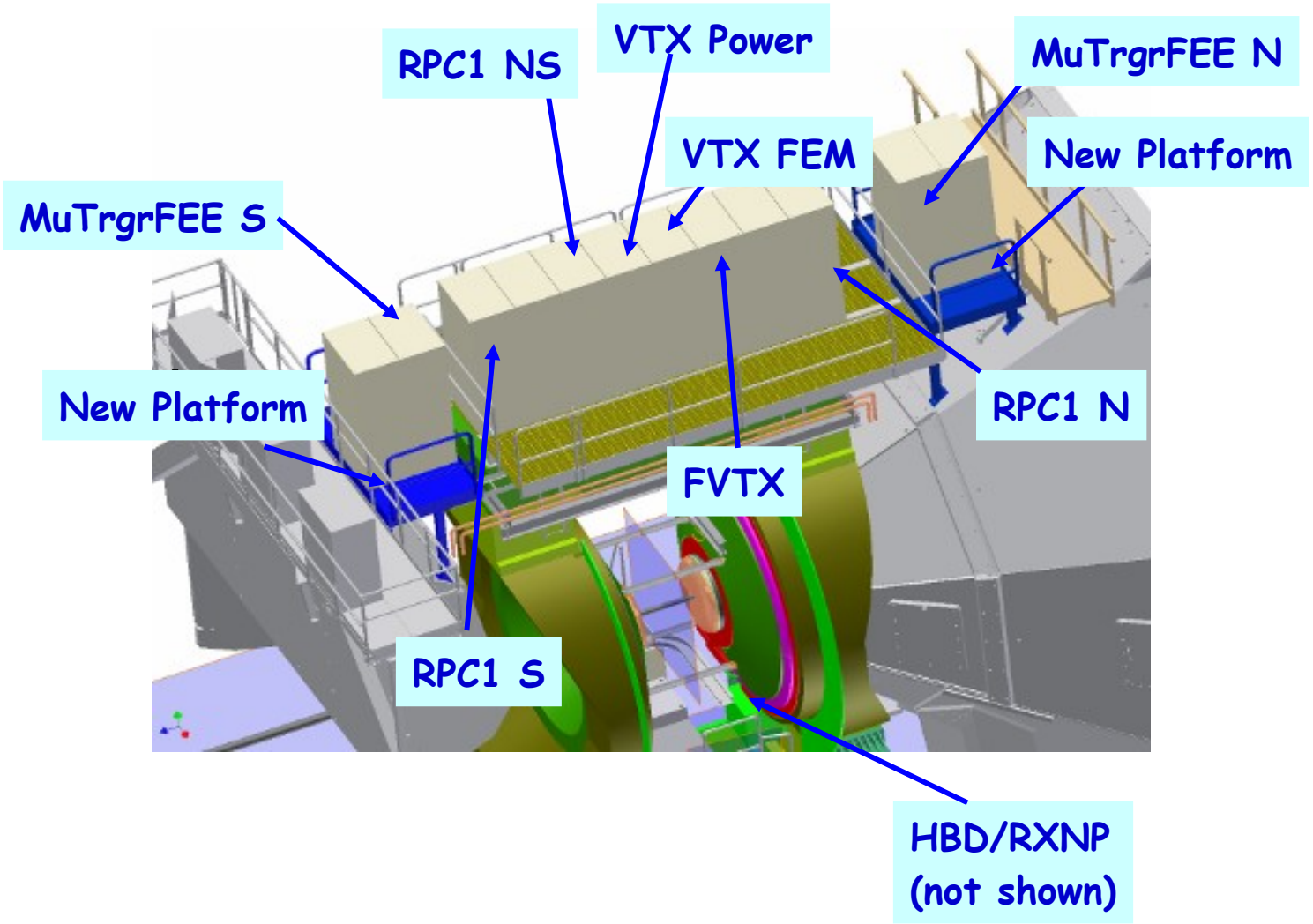
# Power and Ground



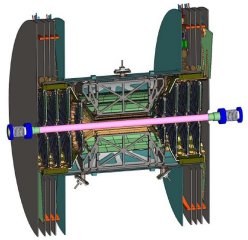


# Rack Allocation in IR



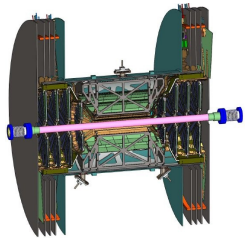


# DCM-2 Status



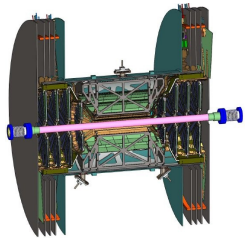
- DCM-2
  - Upgrade to PHENIX DAQ interface.
  - Optical fiber connections.
  - 8/10 bit encoding, 1.6 Gbps.
  - Optical interface complete.
    - Implemented as daughter board using current DCB.
    - Operational for the HBD.
    - Available for system chain test
  - Funding (PHENIX R&D) in place to complete development and design.
  - Design complete 4Q FY09.

# Summary

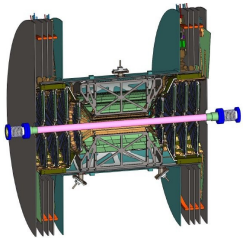


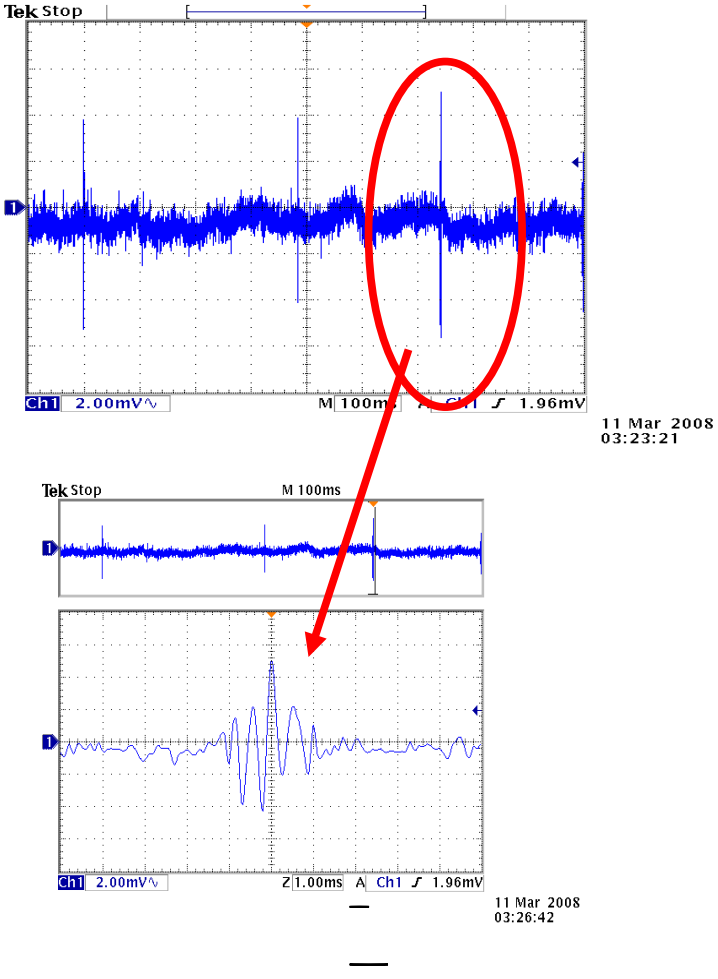
- Review Procedures in place and being implemented.
- Preliminary discussion have occurred with the PHENIX. DAQ/ONCS group to insure seamless integration into PHENIX.
- Grounding plan has been developed for the VTX/FVTX effort.
- Evaluation of power systems has started in conjunction with the VTX group.
- Working with the PHENIX integration group on location of racks, cable routing, patch panels, etc.
- DCM-2 development on track.
- Close communication with FVTX mechanical and integration engineers.

# Backup



# Weiner/ISEG System

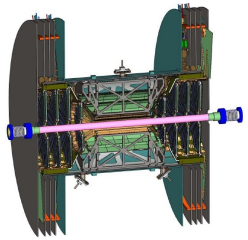






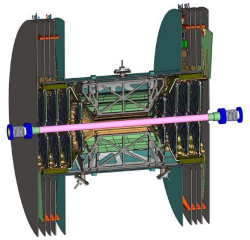
- Low frequency noise, random spikes (2mV p-p)
- High frequency noise, ~70KHz (10mV p-p)
- Tested with prototype 1.5cm pixel ½ ladder
- Meets VTX performance requirements

# Weiner/ISEG System



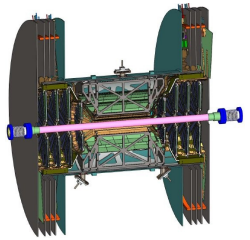
- Electrical Evaluation using VTX Pixel ladders
  - March-May 2008
  - Electrical performance looked acceptable
- Integration Evaluation in 1008 July-September 2008
  - SNMP protocol tested using both Linux and Windows operating systems
  - Basic Linux I/O interface routines written, ISU summer student
  - DAQ/ONCS group concludes that this system will be easy to integrate into PHENIX

# DCM-2



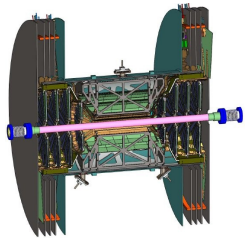
- Collect FEM data
- Zero suppressed data
- Data Error/ Event Alignment checking
  - Alignment checking via L1 data or/and adjacent data link
- Generate PHENIX packet data
- Possibility for data processing
- First stage of event building

# Summary
# WBS 1.8 - Cost and Schedule



- Cost — WBS 1.8.2 $188.1K
- Cost Basis — Labour Rates
- Cost Contingency — 14%
- Schedule — 2Q FY08 – 1Q FY11
- Schedule Contingency — None
- Risk — Low

# Summary
# WBS 1.8 Technical



- Specification Document: TDR
- Workforce (On project):
  - WBS 1.8.2, Electronics Eng. ½ FTE/Year
  - Scope: Duration of project
- Institutions Involved: Columbia/LANL/BNL
- Infrastructure Defined: Draft