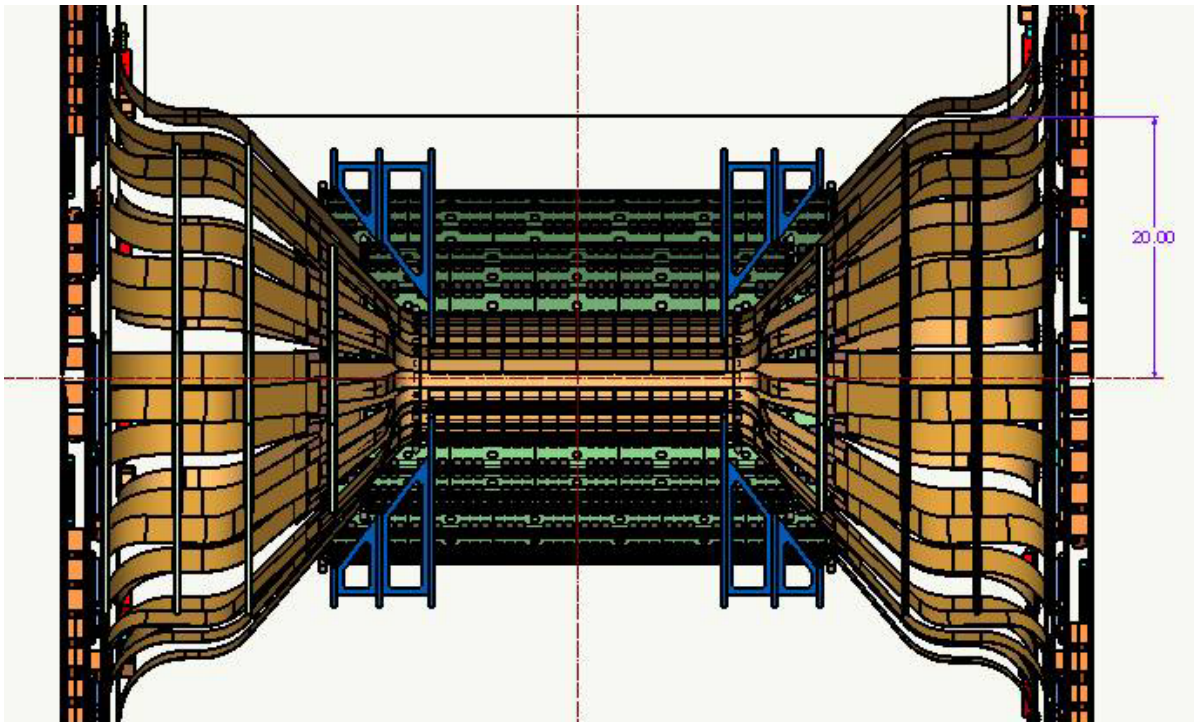
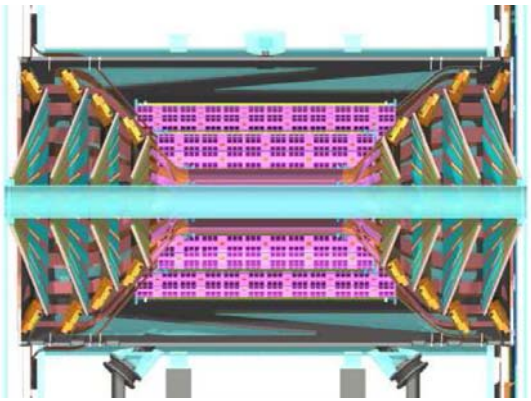
# FVTX Update to VTX

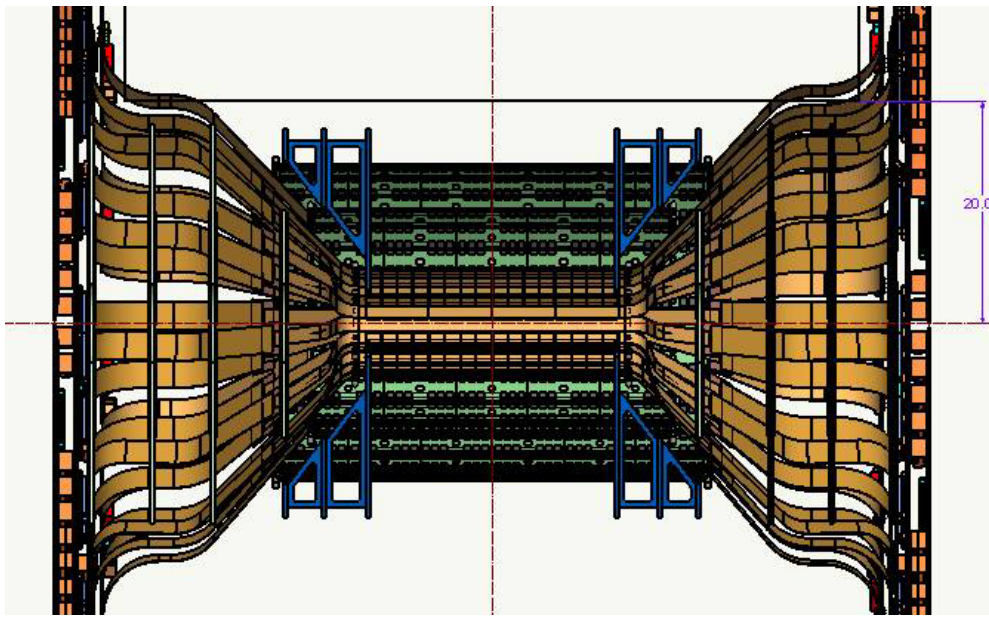
- Detector layout
- Mechanical Work
- Electrical Work
- Simulations
- Getting ready for TDR



# Detector Layout,  Changes

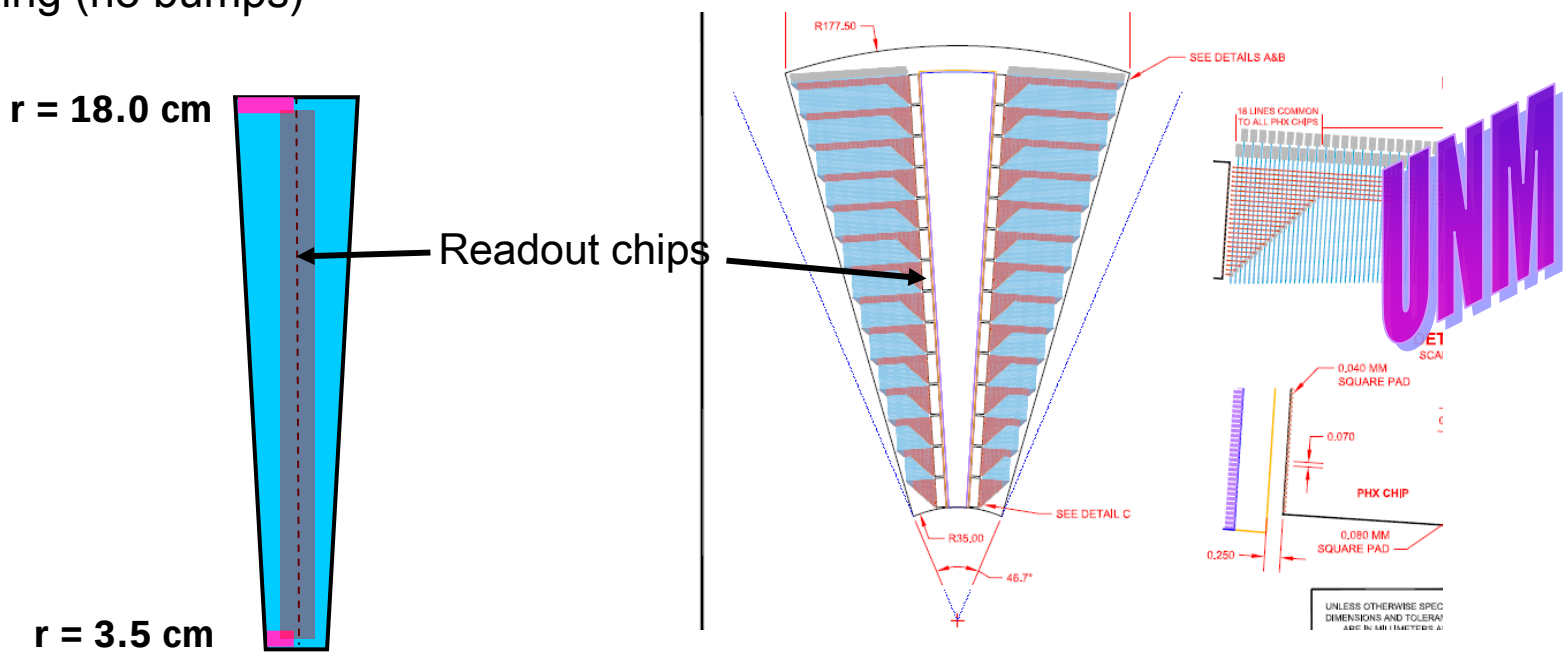
- Vertical layers instead of tilted (mechanical simplicity, increased cluster sizes leads to same or improved performance)
- 75 μm radial pitch instead of 50 μm (useage of clusters reduces strip-width requirement. Occupancy still o.k.), ~3-12mm width in phi
- Still pin-wheel design in each layer, 48 sensors in phi, details of sensor/chip/bus layout changing





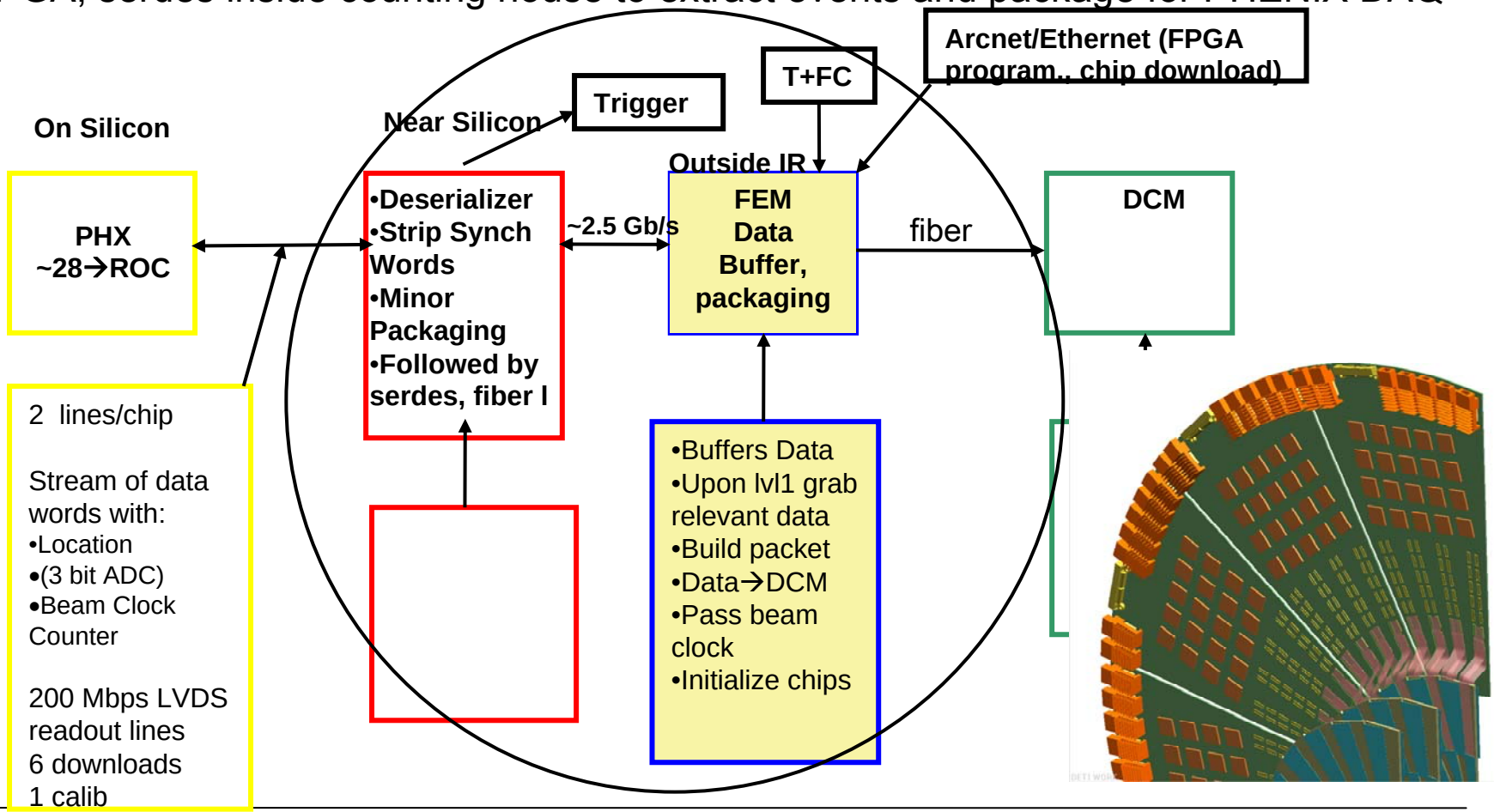
# Sensor/Chip/Bus Layout

- Readout chip down middle of sensor, readout bus underneath to the sides was baseline at last review
- Meetings with FNAL chip designers and UNM (Doug, Martin): too many technical challenges with this layout→chips and bus to side of sensor
- UNM/Dave looking at bus, HYTEC is looking at mechanical implications, FNAL is expecting the baseline chip to be to the side
- Baseline chip: 128 channels per chip, 28 chips per 7.5° wedge in outer layers, wire-bonding (no bumps)



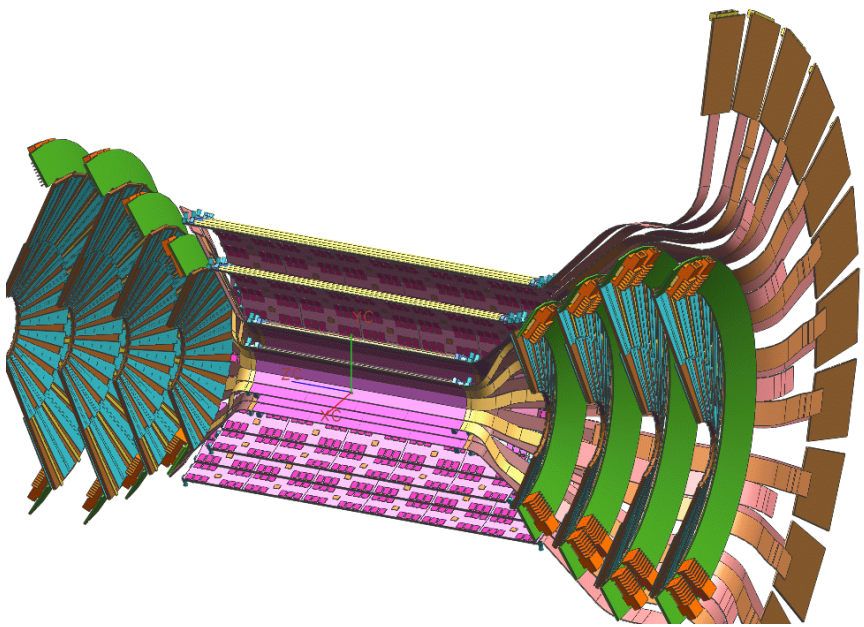
# DAQ Concept

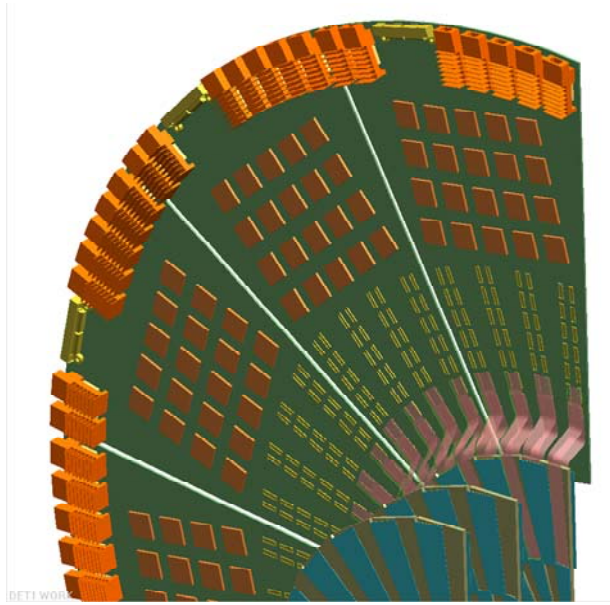
- FPGA, serdes, fiber driver inside enclosure to strip synch words, reduce number of lines out of the enclosure
- FPGA, serdes inside counting house to extract events and package for PHENIX DAQ



# Status of Mechanical and Cooling

- HYTEC work, with Dave, Walt, electrical worker input
  - Update model to see how new wedge layout works
  - Initial look at cooling options (air-cooling unfortunately not feasible even though only ~60 Watts per arm for readout chips)
  - Look at options for location of readout electronics (ruled out option of locating any electronics at ends of sensors, “collars”)
  - Working on layout, power for electronics in “big wheel” (see next)





# Status of Mechanical and Cooling

- HYTEC work, with Dave, Walt, electrical worker input
  - Updating model to see how new wedge layout works

# Status of Sensor/Chip/Bus Work

- Ray Yarema's group at FNAL working on conceptual design of readout chip.
  - Specifications for chip available June '06
  - Completion expected this month. (Jon K. overseeing).
  - Next installation of R+D $ needed to take to layout and prototyping stage.

- Doug and co. (UNM) working with Dave L. on readout bus concepts

- HYTEC looking at mechanical and cooling implications for new layout

- Czech collaborators (Miroslav, Vaclav…) expecting to help with prototype sensors

# PHX Specs, Conceptual Design

"Based on FPIX", but in reality FNAL considers this new design. Analog:

- Collect holes instead of electrons
- Change of amplifier/shaper to handle differing capacitance of strips but retain peaking time within one clock and keep reasonable gain
- Assuming DC-coupled so leakage current compensation circuit must still be present, but some mods to FPIX version needed
- With all changes, still expect to meet noise specs

Data-push architecture retained, but internal logic for getting hits is modified to make simpler to get all hits out fast, modify for different number of channels/chip:

- simpler by linking read clock to beam clock instead of having to assume asynchronous
- Data will always be time-ordered, unlike FPIX
- Can get up to 4 hits/chip out within 4 beam clocks (even AuAu Lvl-1 participation is feasible)
- Data word modified slightly to reflect smaller number of channels, not needing 8 bits for BCO→somewhat smaller

# FVTX Read-out Status: component selection

- Much work by Mark Prokop, EE, LANL to disect radiation environment information and upset/failure rates of various components (took advantage of VTX work)

- Selected Actel, reprogrammable as FPGA of choice in the silicon enclosure

- Working on full component list

- DAQ development at that point continued with Actel for inside IR, Xilinx for FEM using development boards

| | **Actel Axcelerator** | **Actel ProASIC3** | **Altera Stratix II GX** | **Altera Cyclone II** |
|---|---|---|---|---|
| Model | AX 2000 | A3PE3000 | EP2SGX60 | EP2C70 |
| Configuration type | Anti-fuse | FLASH | SRAM | SRAM |
| Radiation Tolerance | 200kRad | 200kRad | 50kRad | 50kRad |
| Single-ended I/O / Differential I/O pairs | 684 / 342 | 616 / 300 | 534 / 78 | 622 / 262 |
| Voltages | 1.5 | 1.5 | 1.2 | 1.2 |
| Power (Quiescent) | 22mA | 25mA | 820mA | 250mA |
| Built-in SERDES | No | No | Yes | No |
| I/O Rates | LVDS - 700 Mb/s | LVDS - 700 Mb/s | LVDS-6.375 Gb/s | LVDS-622 Mb/s |
| Configuration Errors | No | No | Yes | Yes |
| SEE types | clocks, data memory | clocks, data memory | configuration, clocks, memory, SERDES | configuration, clocks, memory |
| SRAM Memory- Data | 294912 | 516096 | 6747840 | 1152000 |
| SRAM Memory- Configuration | 0 | 0 | 16951824 | 14319216 |
| FLASH Memory- Configuration | 0 | 0 | 32 Mbyte | 16 Mbyte |
| RHIC I AuAu SEU Rate - 10 cm /hr-chip | 0.00 | 0.00 | 27.12 | 22.91 |
| RHIC I AuAu SEU Rate - 40 cm /hr-chip | 0.00 | 0.00 | 1.70 | 1.43 |
| RHIC II AuAu SEU Rate - 10 cm /hr-chip | 0.00 | 0.00 | 271.23 | 229.11 |
| RHIC II AuAu SEU Rate - 40 cm /hr-chip | 0.00 | 0.00 | 16.95 | 14.32 |
| RHIC II p+p SEU Rate - 10 cm /hr-chip | 0.00 | 0.00 | 2169.83 | 1832.86 |
| RHIC II p+p SEU Rate - 40 cm /hr-chip | 0.00 | 0.00 | 135.61 | 114.55 |
| Total Integrated Dose | >200k | >200k | >50k | >50k |

# Status of Readout Progress: prototyping ROC+FEM

- Working with FPIX chips, predecessor to our proposed PHX chips

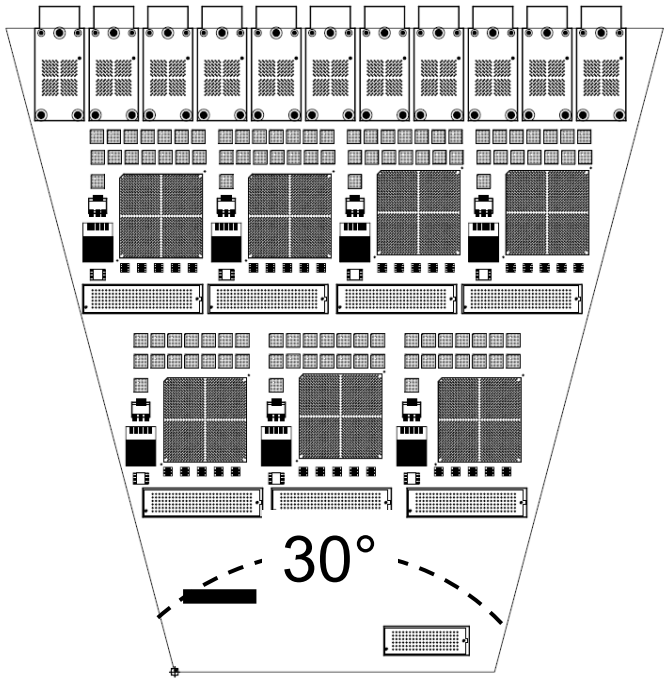
- FPGA connection to chip
  - Successfully reading FPIX chip out, recognizing synch words…
  - Using Actel (reprogrammable), to meet radiation tolerance requirements

- FPGA emulation of FEM
  - Also connecting directly to FPIX chip for now (until Actel interface is complete), with deserializer at the front end
  - Successfully reading in stream of data, parsing into 64 BCO buffers (to allow for 64 clock buffering), taking effective Lvl-1 accept from the chip (got_hit available from chip), and selecting event from relevant BCO

- No show-stoppers found, should work equally well for providing stream to DAQ and future Lvl-1. Details in slow controls, fiber+serdes testing to come.

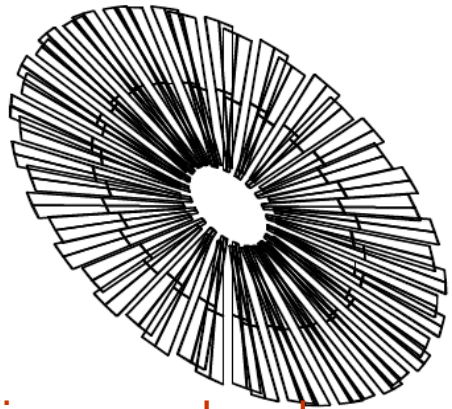
# Status of Readout Progress: layout, power in enclosure

- Components in enclosure:
  - FPGA, serdes, fiber driver, voltage regulators, LVDS repeaters (flash memory)
  - Assume: 28 chips→one ROC, participate in Lvl-1, 2 data lines per chip→56 bundles of 12 fibers out/arm
- Total power expected = ~350 Watts per arm
- Largest component size (z), likely fiber driver = 1.6cm with fins , so 2 cm depth is so far conceivable




- Services four 7.5° wedges
- One layer (of four) shown, with dimensions consistent with current big-wheel

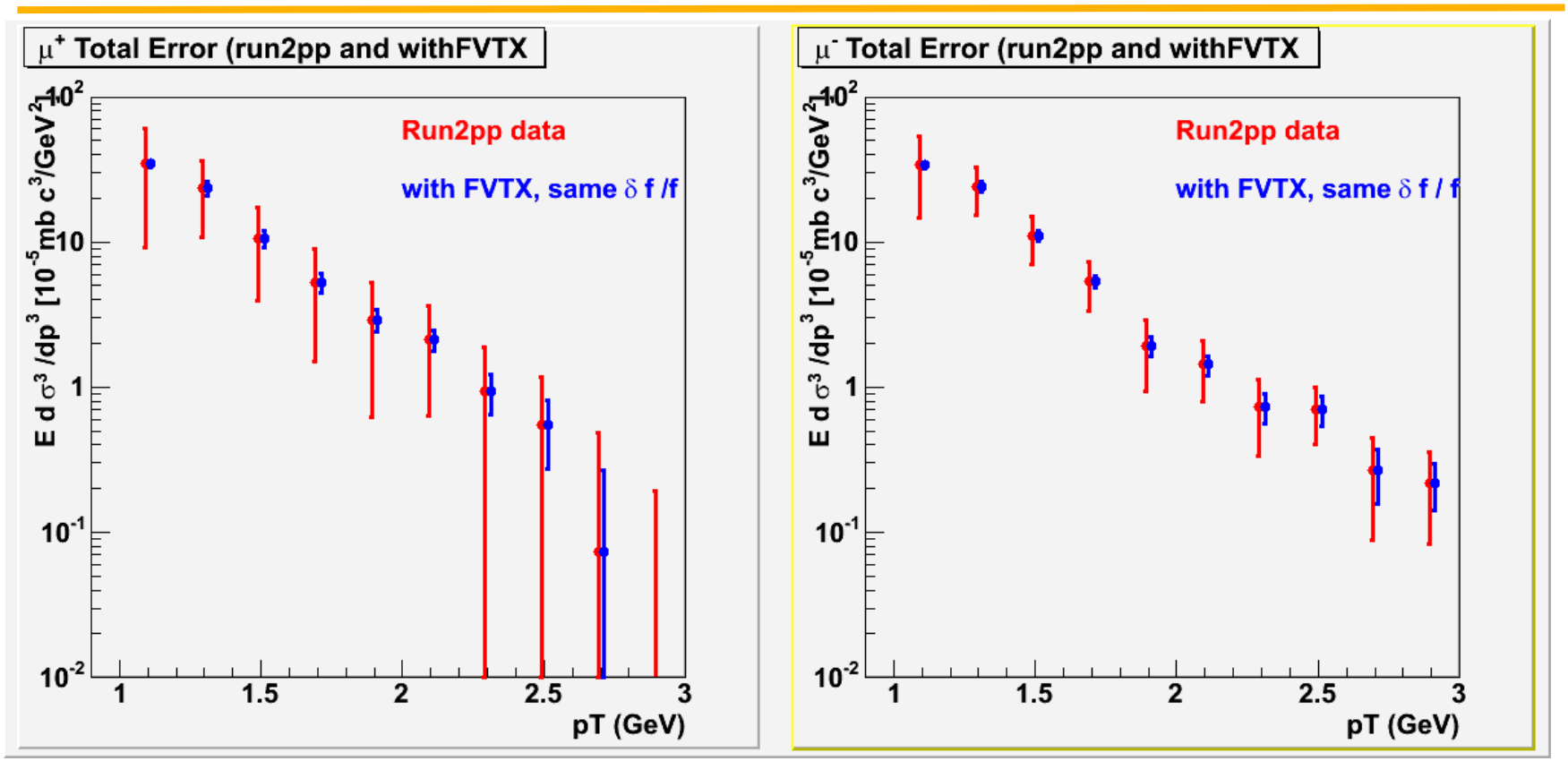
# Simulation Work



- Made list of simulation plots we believe we need :
  - RAA, asymmetry plots… with before and after error bars: Xiaorong already completed first stage
  - Study of separating charm and beauty: UNM working on
  - How can FVTX help background rejection, especially for W physics: Zhengyun studying PYTHIA/PISA currently with Ming
  - All above require better simulations of current detector: FVTX in to offline, Kalman Filter fitter adapted from muon tracker code to FVTX. (Hubert, Hugo, MB,…)
    - Geometry classes completed
    - Option to take pure MC hits, w/, w/out smear, digitize into strips.
    - Option to add VTX hits to tracks/fits
    - To study: geometrical optimization, rejection of unwanted tracks, update signal:background improvement with FVTX…

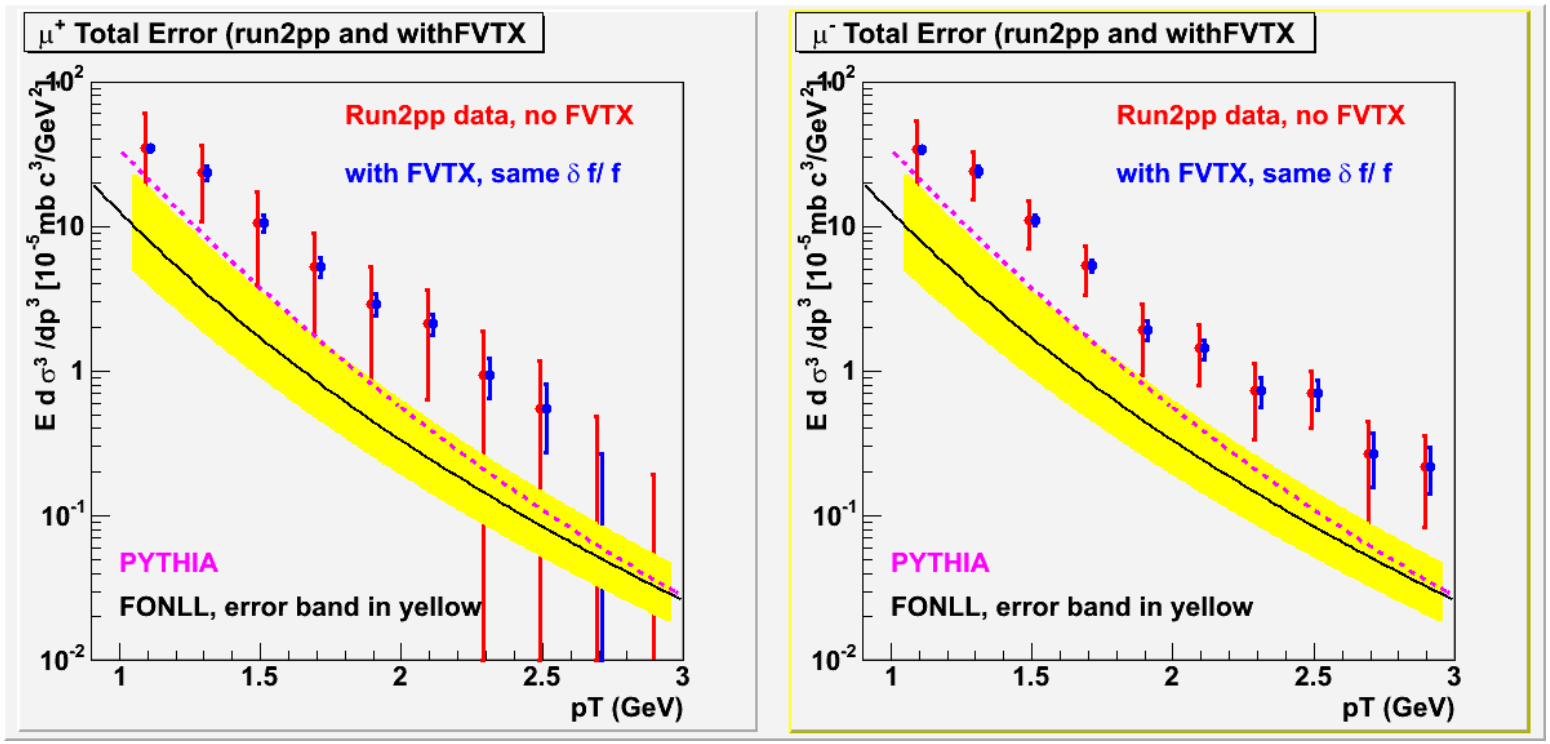
- Plots from Xiaorong, Plots from Zhengyun, Performance Plots…

# Simulation Work – Error Bar Improvements (Xiaorong)



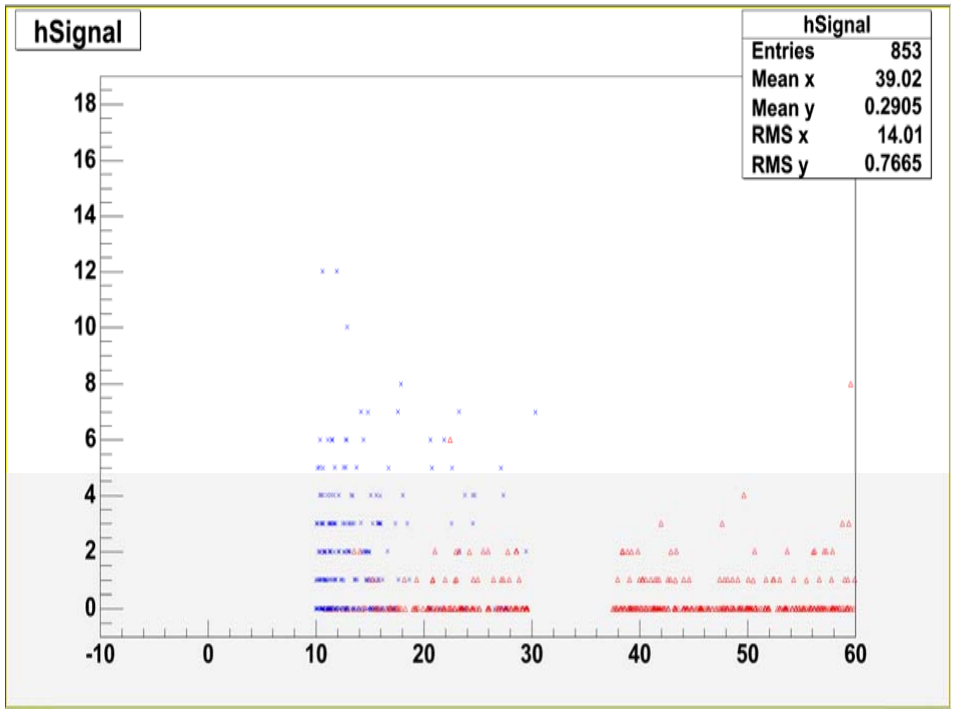

- Example: potential improvement in heavy flavor from single muons.
- Statistical and systematic error improvement
- Spin physics measurement improvements also produced

# Simulation Work – Error Bar Improvements (Xiaorong)

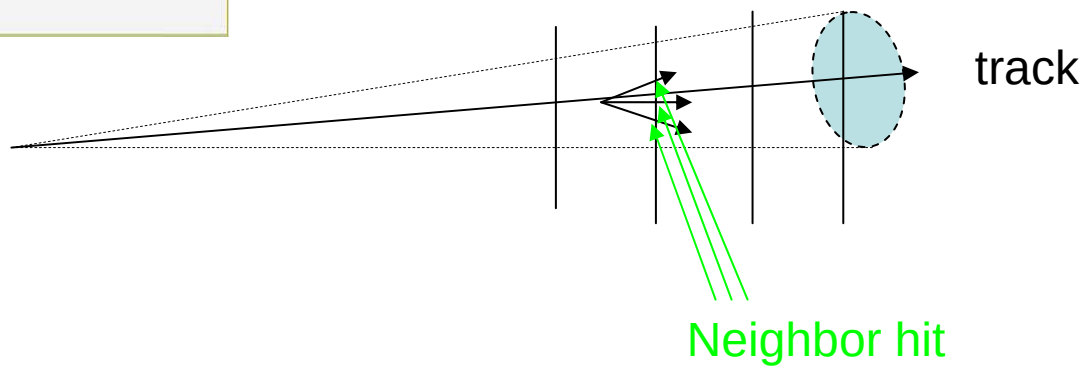



•Working on adding model comparisons to physics plots to show how we can/cannot distinguish various models with/without the FVTX

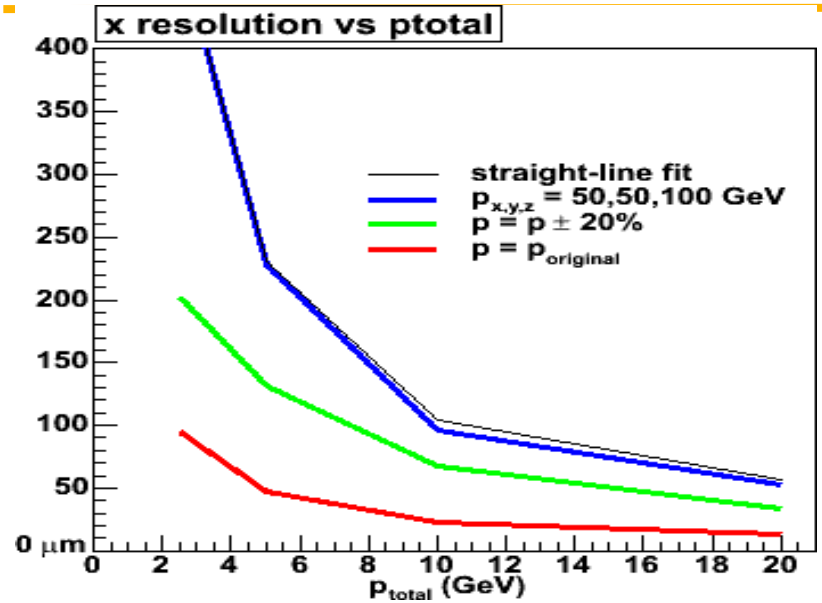
# Simulation Work – W Measurements



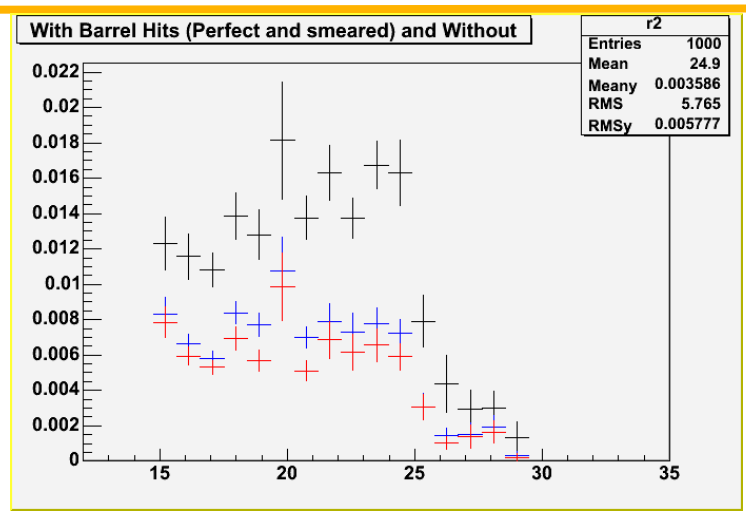

Can FVTX used for isolation cut to improve W signal:background?



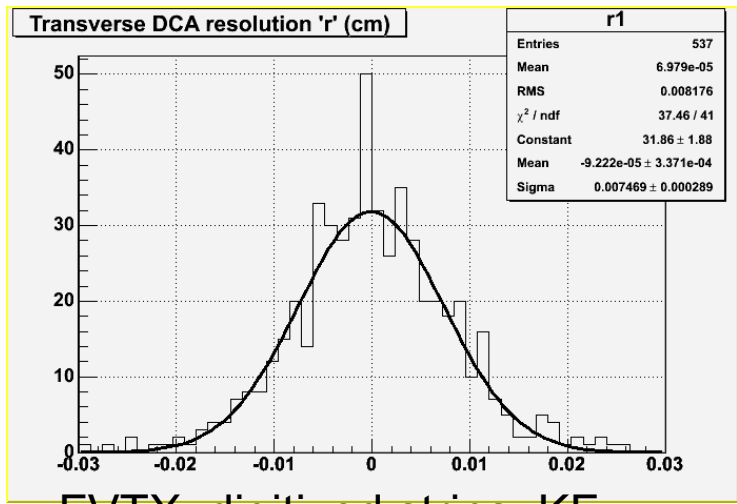
# Simulation Work – KF Resolutions in Progress




Straight-line fit compared to KF, "perfect", and if some momentum knowledge




With/Without VTX




FVTX, digitized strips, KF

# Near Future Work

- Updating FVTX Proposal, with plan to have an update available by January
- Working, especially, to address all past review comments
- Expecting DOE review spring/early summer
- Critical Path:
  - PHX design (FNAL started)
  - Sensor design (Czech expect to help as soon as PHX settled, about now)
  - Mechanical work, in terms of answering past review issues
  - Simulation work, in terms of getting ready for review
  - DAQ well underway, but need to get details for inside enclosure before it is set in stone

# Backups

# Addressing other review comments, DOE requirements

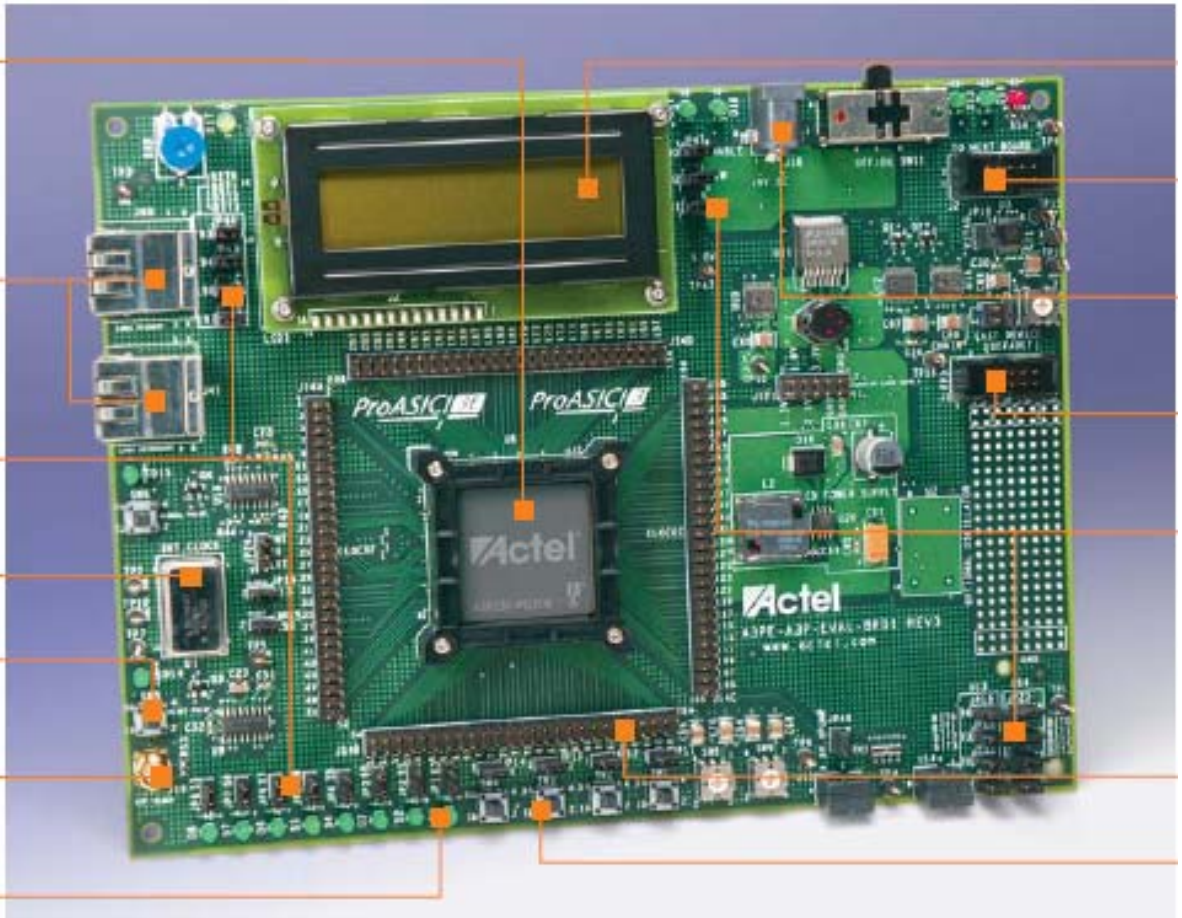
Requirements for MIE construction start in FY2008:

- R&D issues resolved ( see FVTX Milestones)
- Technical Proposal to BNL – Jan 2007
    - Responses to Mar 2006 TAC Committee recommendations
    - complete cost and schedule update reflecting technology choices
- Formal Management Plan ~1/2 done
- Workforce spreadsheets will be prepared.
- DOE readiness review ~ late spring 2007
- FVTX responds to DOE review recommendations

Some of the Review Questions to be addressed:

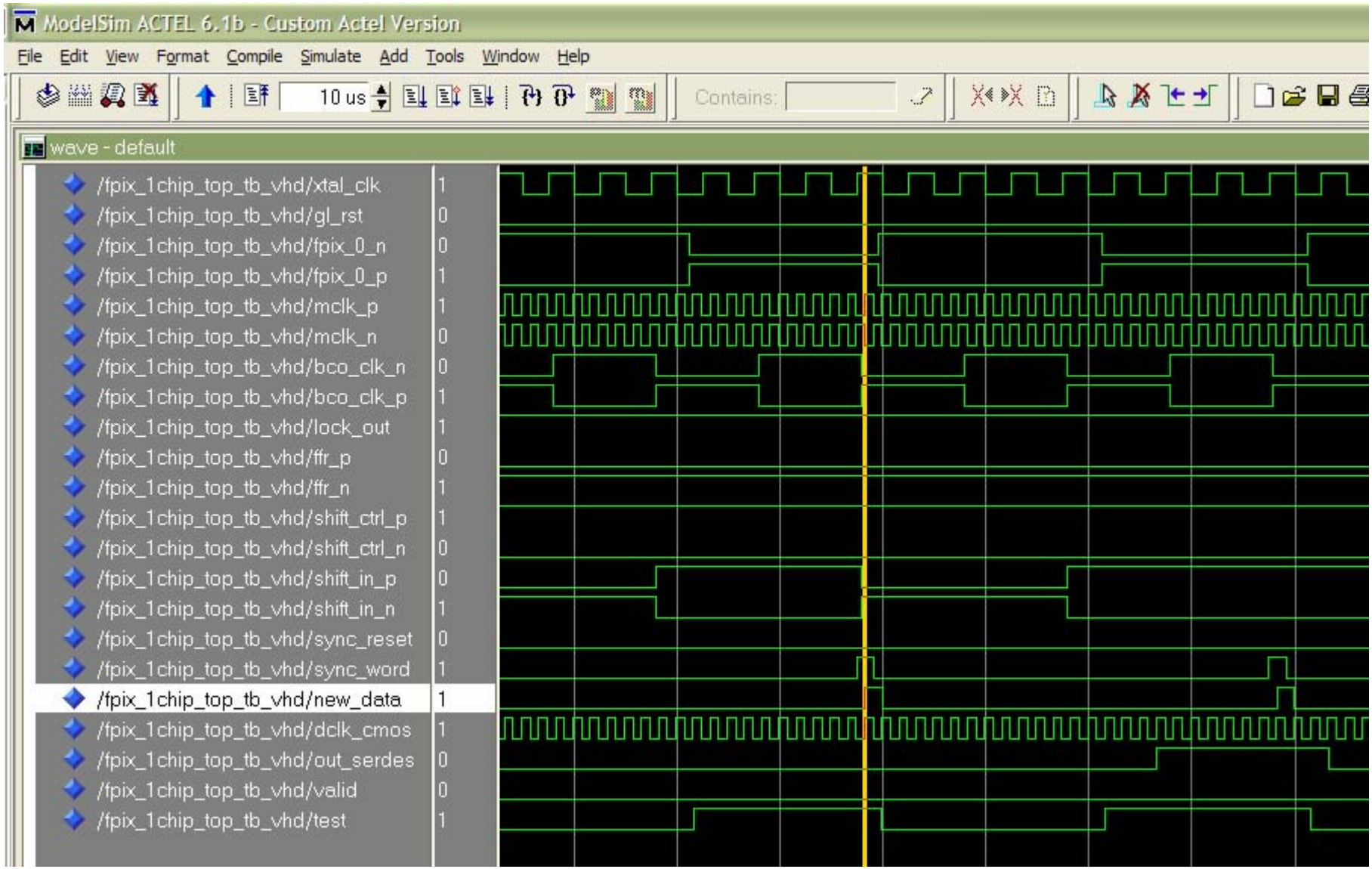
- Physics simulations (see previous)
- Want more final chip-sensor design: FNAL PHX development starting, Czech collaborators to work with us on prototype sensor
- Tighter coupling with FNAL on their work: Jon K. to work 50% on oversight…
- Want more mechanical work up front: came up with LANL$ to start HYTEC work this FY
- Questions on cost and schedule will be addressed with updated cost and schedules

# Actel ProASIC3 Starter Board



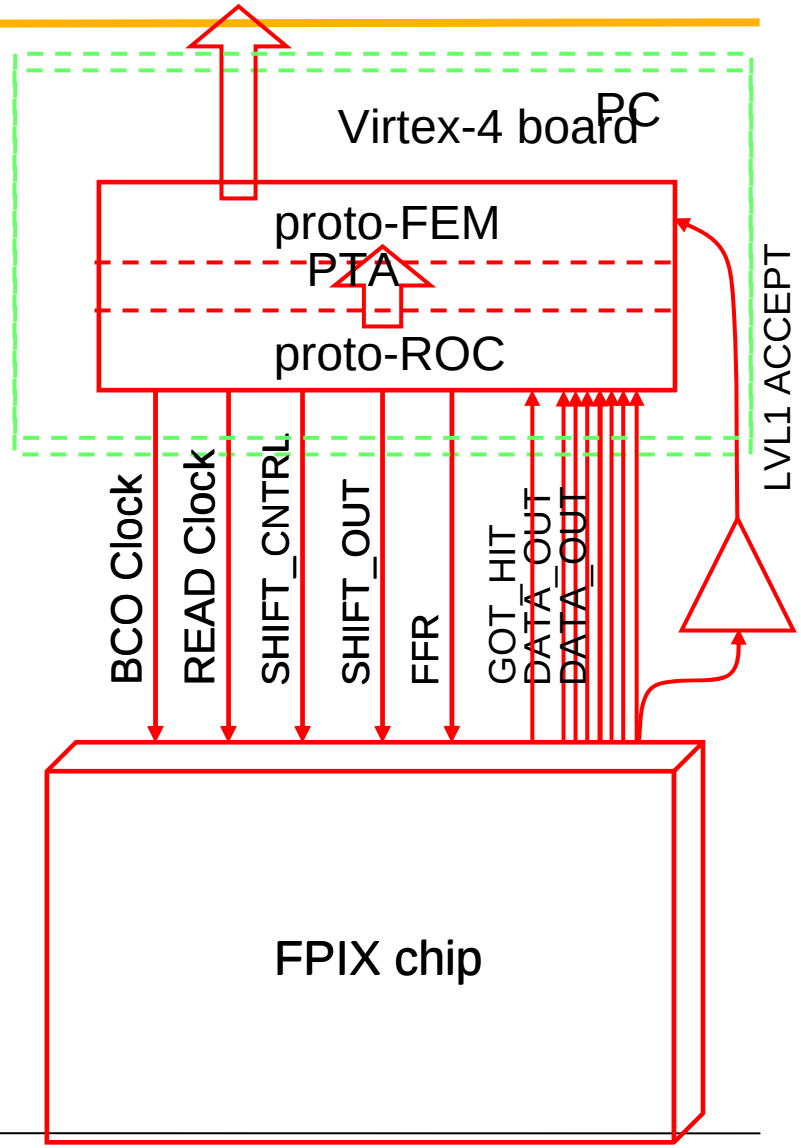

- Flash FPGA A3P250 in 208 pin package.
- 34 LVDS I/O pairs.
- In theory all pins can be accessed.
- In practice only 7 LVDS I/O pairs can be used reliably.
- Lots of undocumented features like IO banks fixed to 3.3 V, preventing LVDS usage etc.

# Simulation

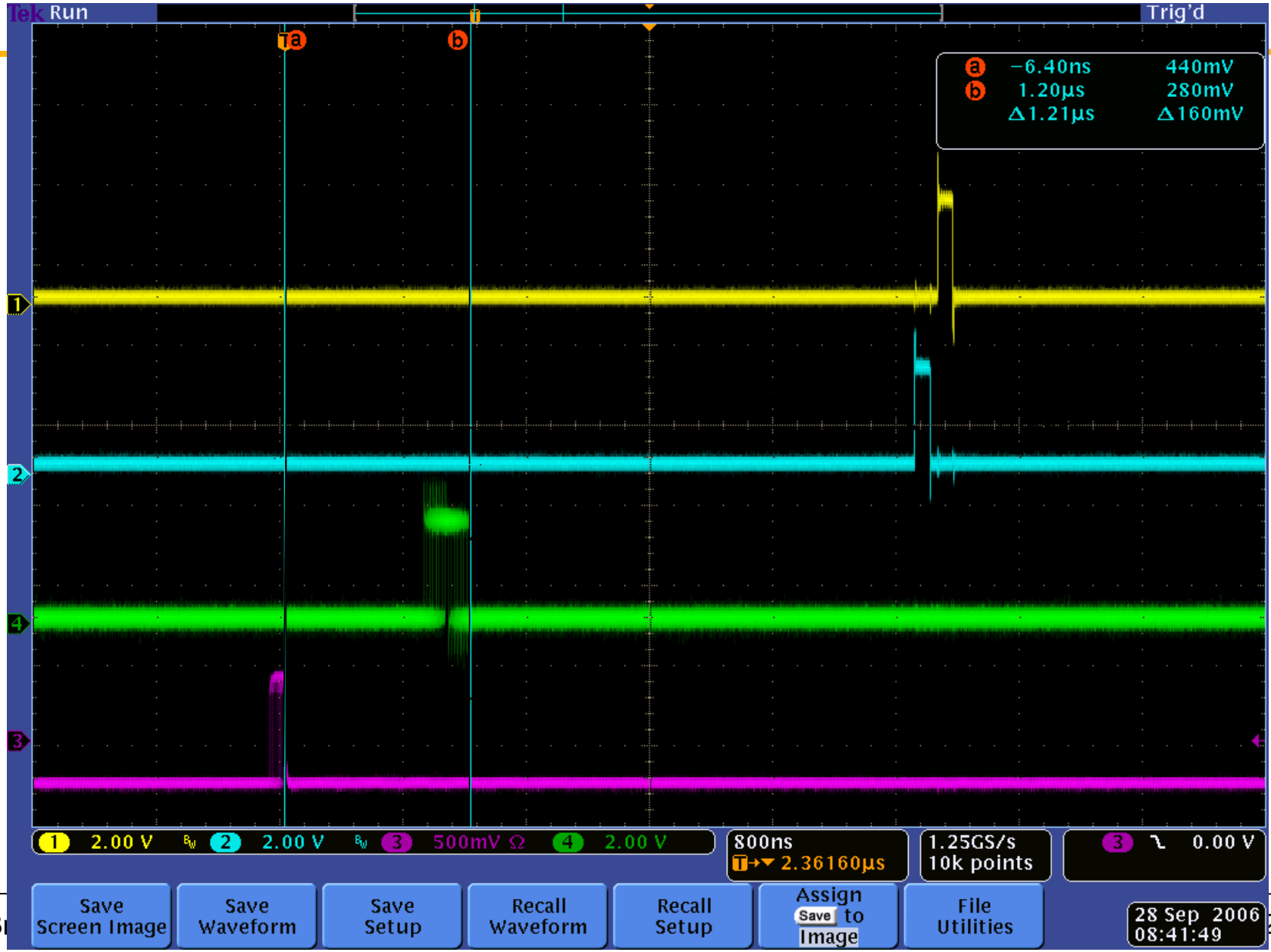
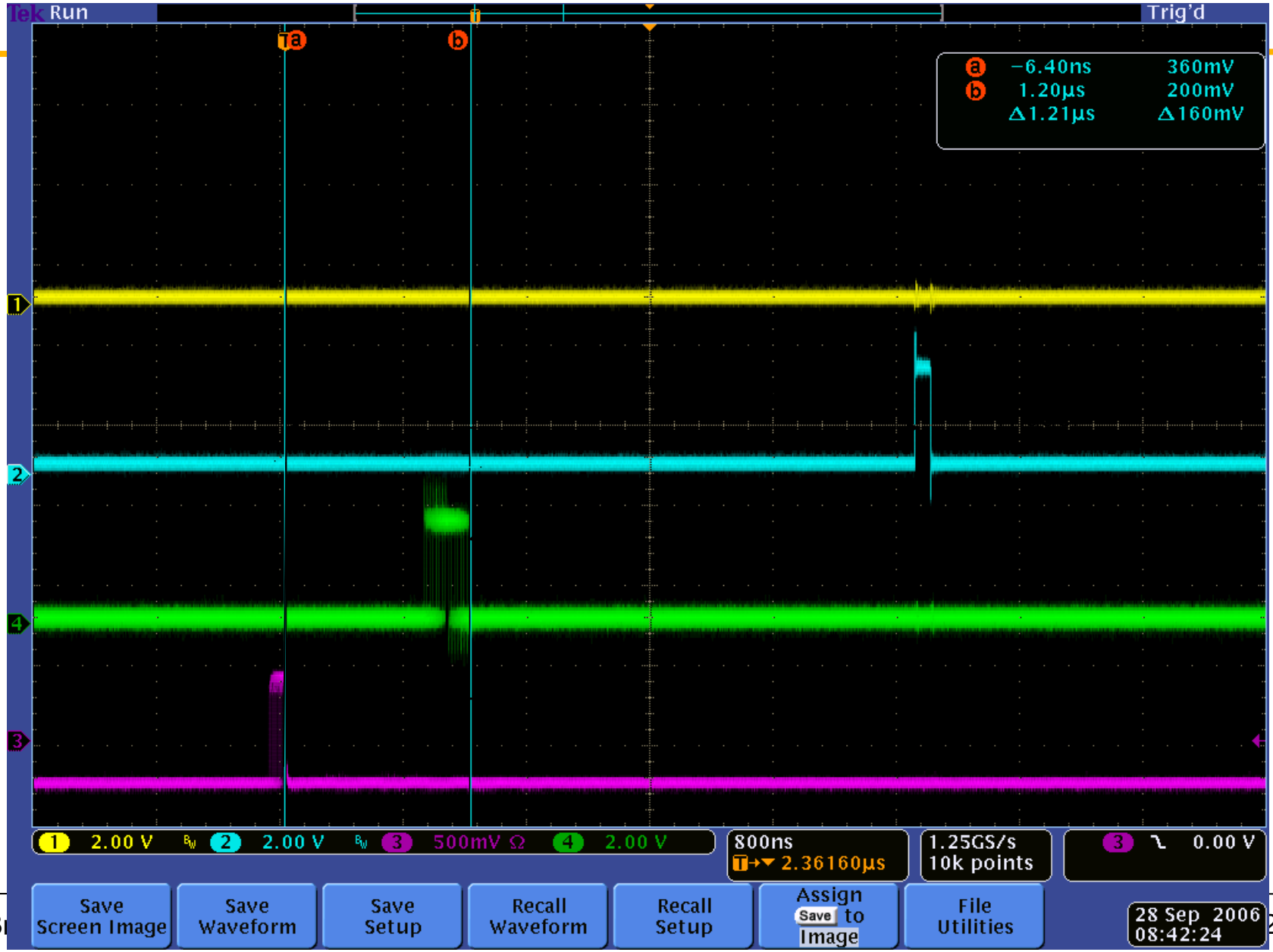

ModelSim ACTEL 6.1b - Custom Actel Version
File Edit View Format Compile Simulate Add Tools Window Help
10 us
Contains:
wave - default
/fpix_1chip_top_tb_vhd/xtal_clk 1
/fpix_1chip_top_tb_vhd/gl_rst 0
/fpix_1chip_top_tb_vhd/fpix_0_n 0
/fpix_1chip_top_tb_vhd/fpix_0_p 1
/fpix_1chip_top_tb_vhd/mclk_p 1
/fpix_1chip_top_tb_vhd/mclk_n 0
/fpix_1chip_top_tb_vhd/bco_clk_n 0
/fpix_1chip_top_tb_vhd/bco_clk_p 1
/fpix_1chip_top_tb_vhd/lock_out 1
/fpix_1chip_top_tb_vhd/ffr_p 0
/fpix_1chip_top_tb_vhd/ffr_n 1
/fpix_1chip_top_tb_vhd/shift_ctrl_p 1
/fpix_1chip_top_tb_vhd/shift_ctrl_n 0
/fpix_1chip_top_tb_vhd/shift_in_p 0
/fpix_1chip_top_tb_vhd/shift_in_n 1
/fpix_1chip_top_tb_vhd/sync_reset 0
/fpix_1chip_top_tb_vhd/sync_word 1
/fpix_1chip_top_tb_vhd/new_data 1
/fpix_1chip_top_tb_vhd/dclk_cmos 1
/fpix_1chip_top_tb_vhd/out_serdes 0
/fpix_1chip_top_tb_vhd/valid 0
/fpix_1chip_top_tb_vhd/test 1

# Readout Progress -- FEM

- Current readout scheme
- Need to design triggered readout, implementing the main components of ROC and FEM
- Simple solution:
  - Use GOT_HIT, delayed by "X" BCO clocks as a "self-trigger"
  - Implement deserializer, initializer, FIFO array on Virtex-4 evaluation board
- Read the correct bucket of data upon "self-trigger" signal arrives



# Timing diagram, correct RF bucket



# Timing diagram, incorrect RF bucket