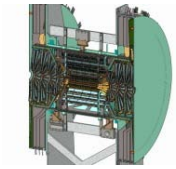
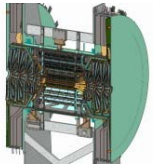


Sensors/FPHX Readout Chip

WBS 1.4.1/1.4.2

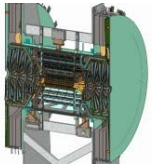
Jon S Kapustinsky



Outline

- Overall design of the FVTX wedge and FPHX readout chip
- Silicon sensor specifications and tests
- FPHX specifications and tests
- FVTX wedge system tests
    - Pulser
    - Beam
    - Cosmic ray
- Schedule

Design Decisions Leading to the FVTX Sensor Wedge and FPHX

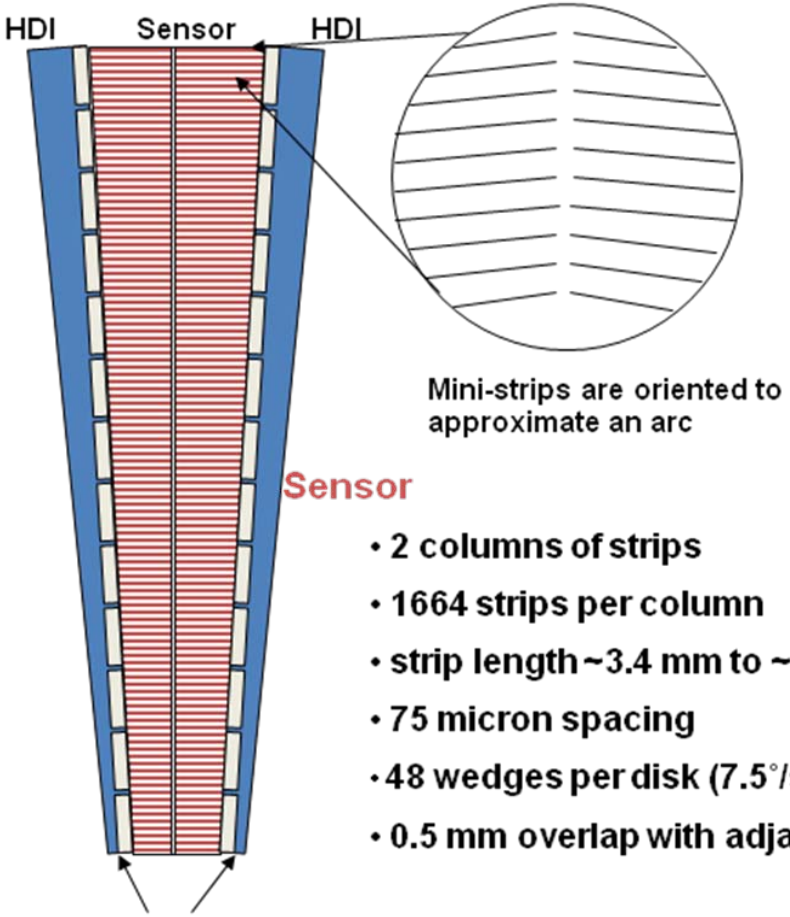


Technical risk minimization the key driver

- **Mini-strips maintain good resolution in r and phi with reasonable occupancy and manageable channel count**
- **Wire bonds replace initial idea to use bump bonds**
- **Chip placement moved from centerline of sensor to the edges**
  - **minimizes potential noise coupling between chip and sensor**
  - **facilitates implementation of decoupling between sensor bias and chip reference and avoids long path-length sensor return to ground**

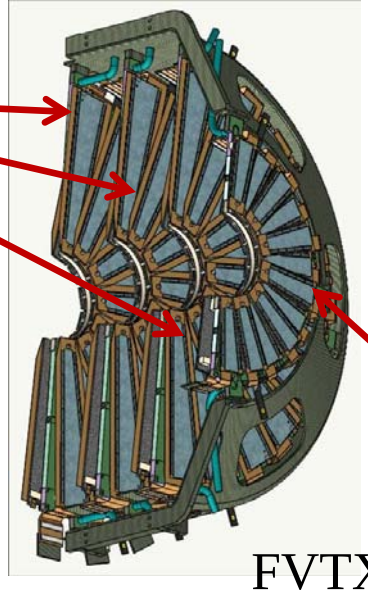
- **Wedge assembly unit based on ease of assembly**
- **Readout architecture of the FPHX draws on previous successful designs; FPIX2, FSSR, and the SVX family of readout chips (0.25 micron TSMC CMOS process)**
- **Low power design of the FPHX simplifies cooling and mechanics significantly**

FVTX Sensor Long Wedge

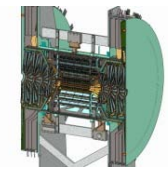


- 2 columns of strips
- 1664 strips per column
- strip length ~3.4 mm to ~11.5 mm
- 75 micron spacing
- 48 wedges per disk (7.5°/sensor, 15°/wedge)
- 0.5 mm overlap with adjacent wedges

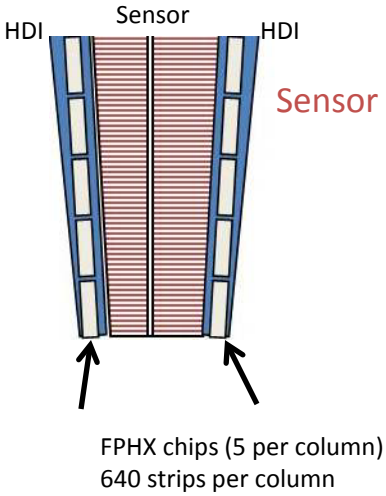
Overall length 126.8 mm
Overall width 8.8 mm i.r., 25.4 mm o.r.



4 hermetic disks, z =18.5 to 38 cm

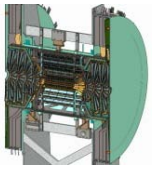


FVTX Sensor Short Wedge

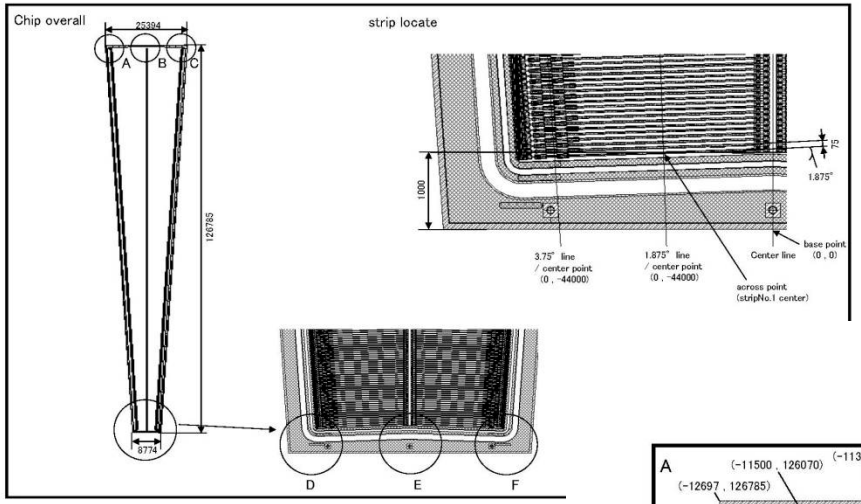


Overall length 50.1 mm
Overall width 8.8 mm i.r., 15.3 o.r

FVTX Sensors



Novel design places two independent sensors on one substrate



p-implant on n-bulk
ac-coupled
1.5 MΩ polysilicon bias resistors
Depletion voltage < 100V
75 micron pitch

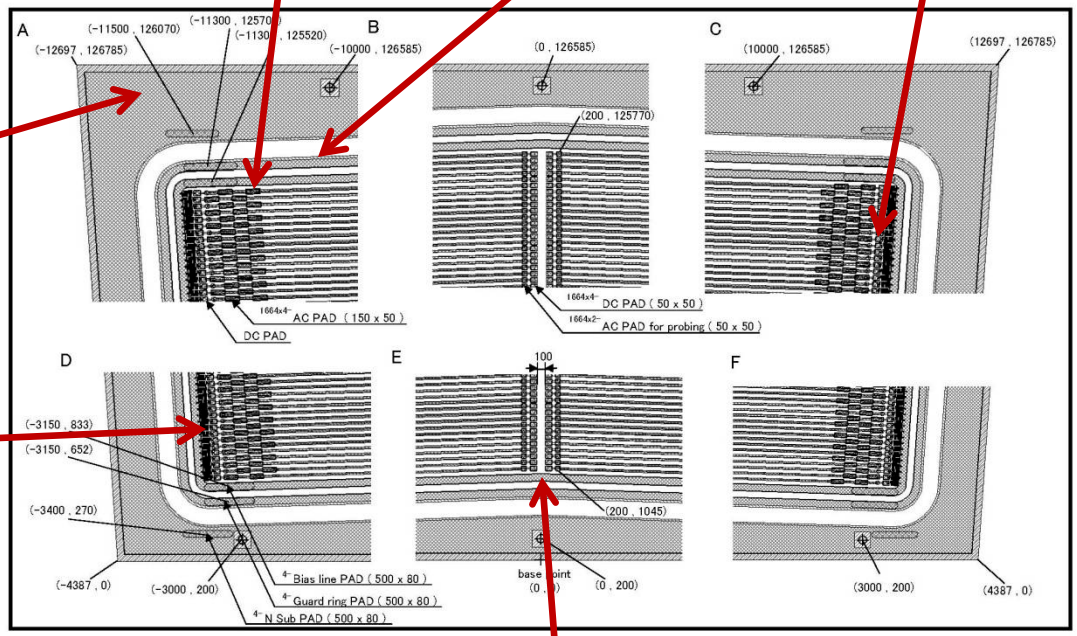
P-Bias Ring

P-Guard Ring

Double Bond-Pad Rows

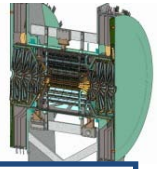
N-Surround

Polysilicon Bias Resistors

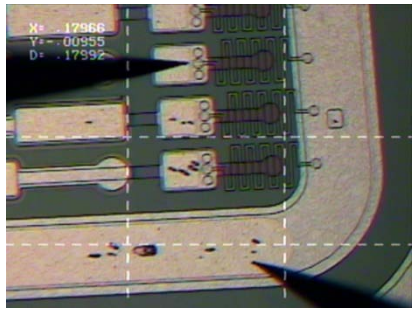


100 micron gap

QA Silicon Sensor Wedges (UNM, Prague, LANL)



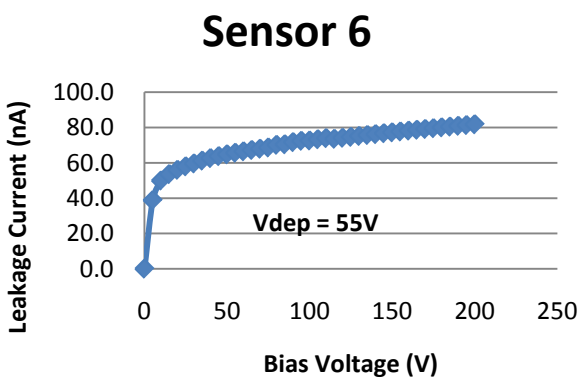
QA specifications



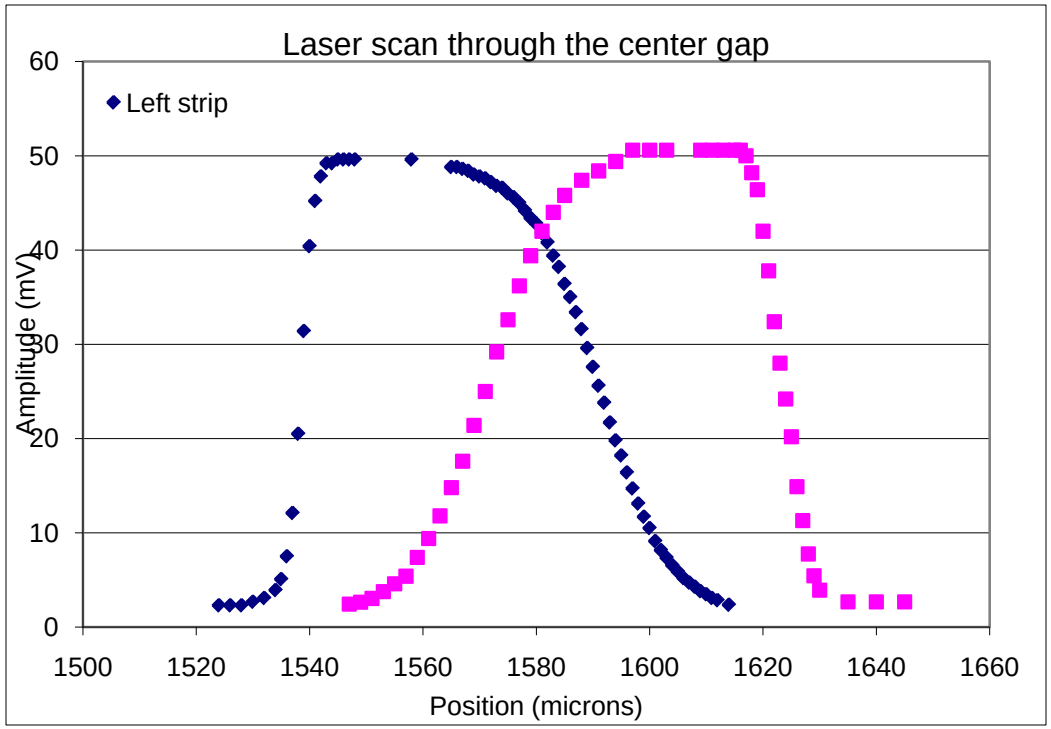
- Visual inspection to identify processing or handling flaws
- Current versus voltage characteristic curve for each sensor
- Full depletion voltage and breakdown voltage for each sensor

Sensors delivered from Hamamatsu are fully tested

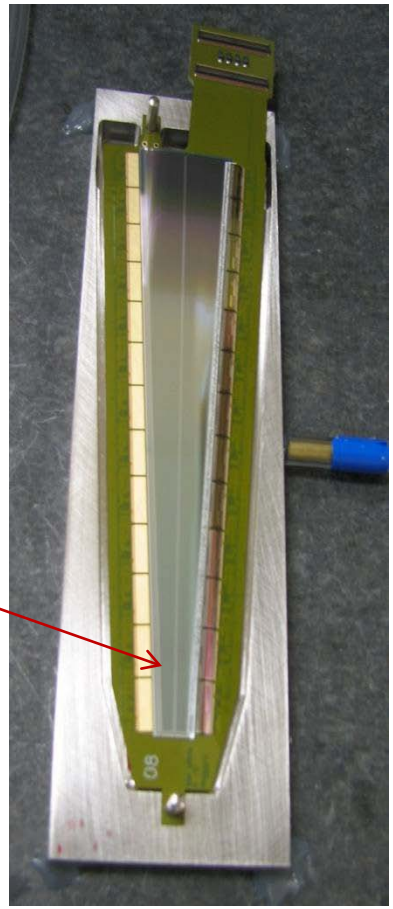
- Coupling capacitor integrity or short for each strip
- Implant open or short for each strip
- Polysilicon resistor open or short for each resistor



Laser Tests on silicon sensor at UNM



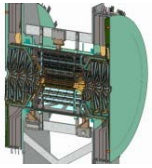
The 1064 nm laser was used to scan the 100 micron gap between left and right strips in steps of 1-to-5 microns.



*** Only one probe is used, so each strip is measured with the coupling capacitor on the other strip not connected. All strips, however, are dc connected to ground through the polysilicon resistors.**

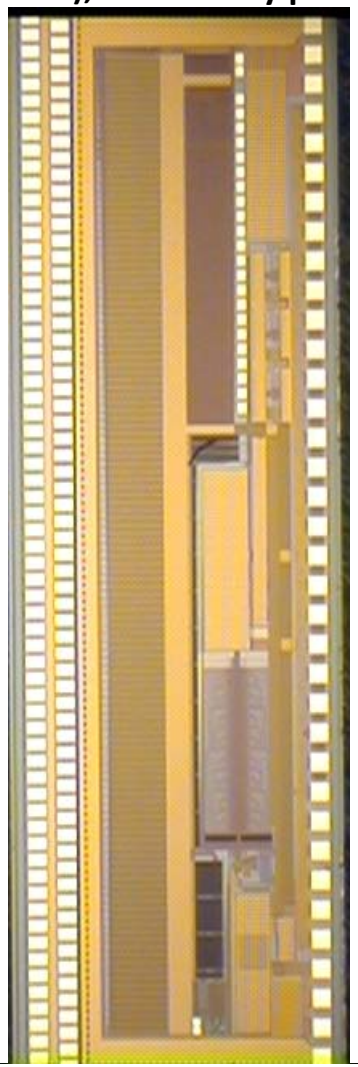
Amplifier/Probe to measure charge

The FPHX Chip

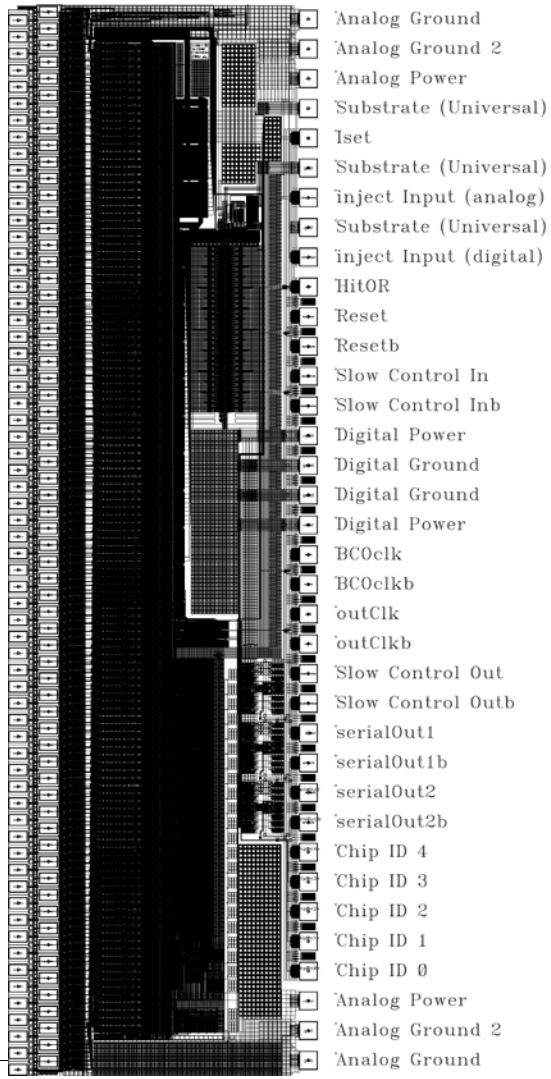


The FPHX is the custom readout chip designed for the FVTX Silicon Sensor. Each FPHX chip integrates and shapes (CR-RC) signals from 128 channels of mini-strips, digitizes and sparsifies the hit channels each beam crossing (106ns beam clock), and serially pushes out the digitized data.

Photo

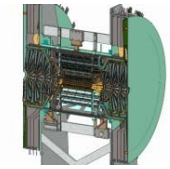


Layout

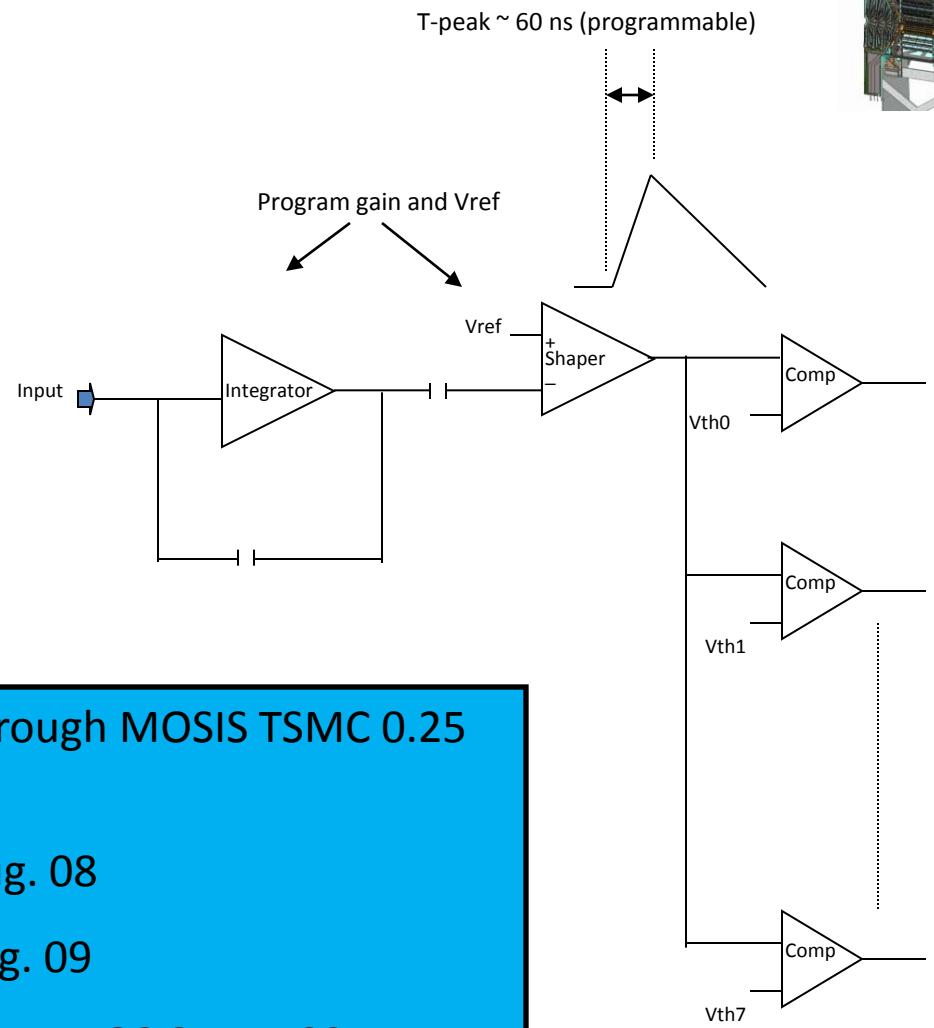


The FPHX is a mixed-mode chip with two major and distinct sections, the front-end and the back-end.

FPHX readout chip front end



- 128 channel
- 46 to 200 mV/fC
- 60 ns peak time (programmable)
- 3—bit ADC (programmable)
- Optimized for 1 to 2.5 pf
- 115e + 134e/pf
- ~ 70 to 140 uW/ch (dep. Bias current)



Programmable Thresholds

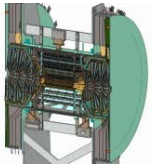
Fully functional chip design submitted through MOSIS TSMC 0.25 micron process

FPHX1 delivered Aug. 08

FPHX2 delivered Aug. 09

FPHX Production Chip submitted to MOSIS Nov. 09

Front-end Specifications



Configuration: 128 identical channels. Each channel contains a charge integrator, shaper, programmable threshold discriminator, and an 8-comparator thermometer ADC with fully programmable thresholds.

Input charge signal polarity: positive (holes)

Input capacitance: the design is optimized for an external detector capacitance of approx. 1.5pF (and estimated chip parasitic C of 0.5pF)

Detector leakage current compensation: programmable maximum of 0 – 100nA

Effective Channel gain: 46, 50, 60, 67, 85,100, 150, or 200 mV/fC (programmable)

Output: 3-bit digital code per channel (digitized shaper output pulse height). No analog output.

Output pulse dynamic range (shaper output): >800mV (25ke to 100ke, depending on the gain setting)

Nominal output pulse peaking time: 60 ns (programmable, set by the shaper)

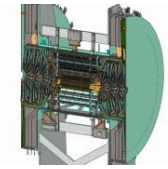
Output pulse fall time: programmable, set by the integrator fall time adjust

Noise at shaper output: 115e + 134e/pf (simulation)

Power: Approx. 140 uW per channel for the maximum input transistor bias current of 38uA, approx. 300 uW per channel for the back end.

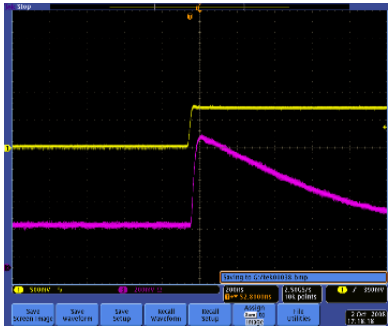
2 test pulse inputs: one direct analog, one controlled by a DAC and digital input.

FPHX1 Programmable Bits – Gain, Fall time, Rise time (LANL)

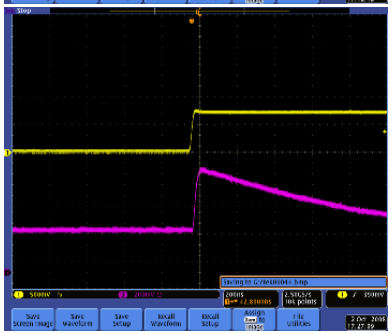


- The shaper output saturates at approximately 800 mV
  - At a gain of 50 mV/fC dynamic range is 16 fC (~4 MIP's)
  - Most probable input charge is ~ 2fC

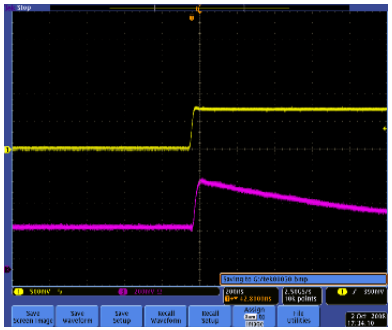
Gain



100 mV/fC

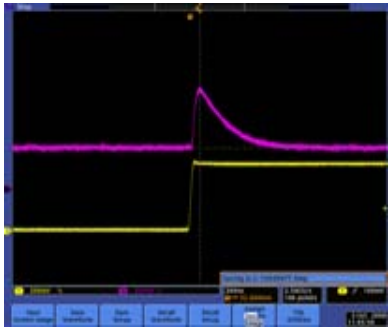


66 mV/fC

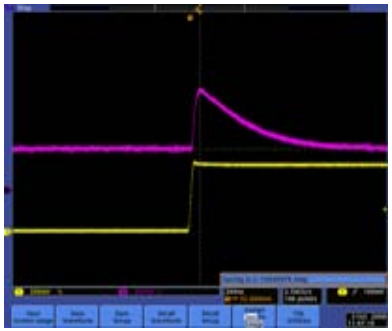


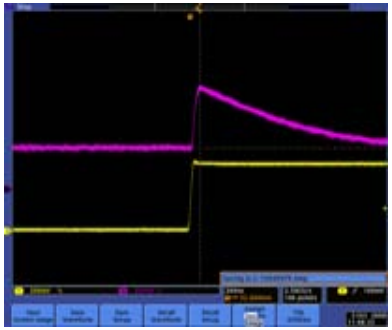
50mV/fC

Fall time



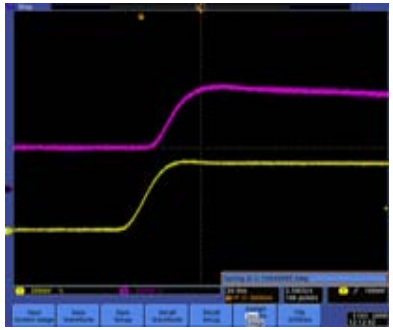
Fast
~250 ns



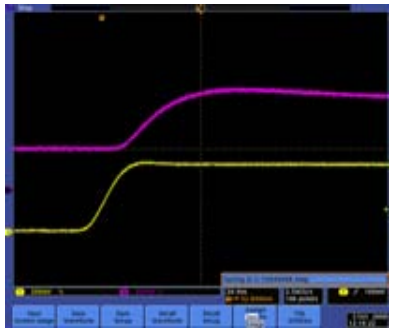


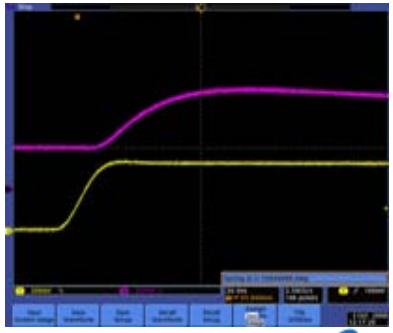
Slow
~2 µs

Rise time



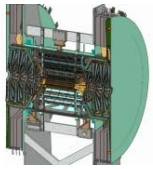
30 ns





90 ns

FPHX Chip back-end organization



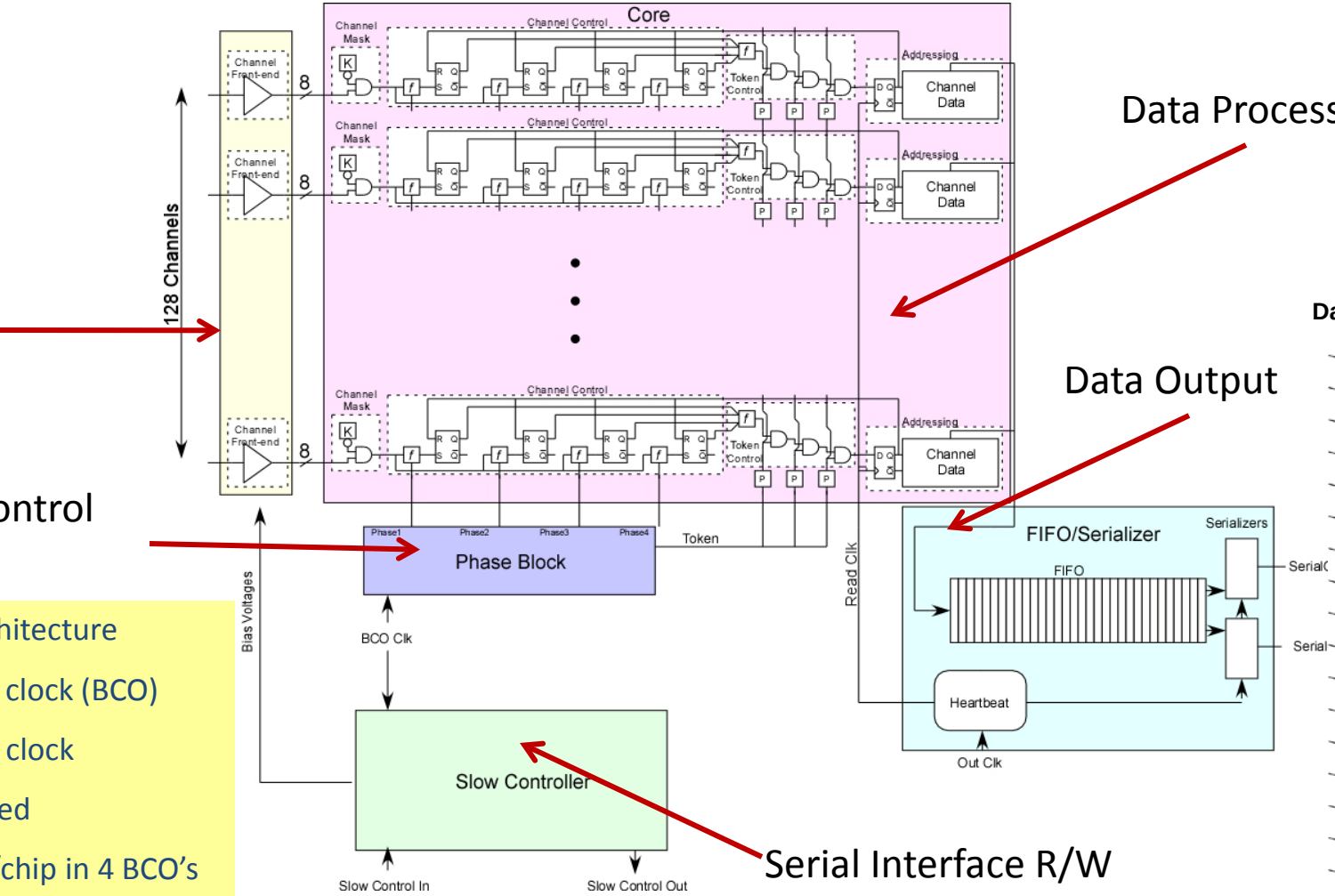
Data Processing

Analog

Phase Control

Data Output

Serial Interface R/W



Data push architecture

10 MHz beam clock (BCO)

200 MHz data clock

Zero suppressed

Output 4 hits/chip in 4 BCO's

Approx. 300 uW/ch

Slow Control Word

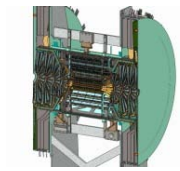
32 bits

1	1	0	0	1	1	1	C_4	C_3	C_2	C_1	C_0	0	0	0	0	1	I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	0*	0	0	0
Header 0	Header 1	Header 2	Header 3	Header 4	Header 5	Header 6	Chip ID 4	Chip ID 3	Chip ID 2	Chip ID 1	Chip ID 0	Reg Addr 4	Reg Addr 3	Reg Addr 2	Reg Addr 1	Reg Addr 0	Instruction 2	Instruction 1	Instruction 0	Ch Addr 7	Ch Addr 6	Ch Addr 5	Ch Addr 4	Ch Addr 3	Ch Addr 2	Ch Addr 1	Ch Addr 0	Trailer 3	Trailer 2	Trailer 1	Trailer 0

Data Word

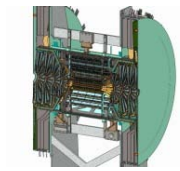
FIFO Full	b_{19}
Magnitude[2]	b_{18}
Magnitude[1]	b_{17}
Magnitude[0]	b_{16}
Word Mark	b_{15}
Location[6]	b_{14}
Location[5]	b_{13}
Location[4]	b_{12}
Location[3]	b_{11}
Location[2]	b_{10}
Location[1]	b_9
Location[0]	b_8
Time[6]	b_7
Time[5]	b_6
Time[4]	b_5
Time[3]	b_4
Time[2]	b_3
Time[1]	b_2
Time[0]	b_1
Sync Bit	b_0

Back-end Features

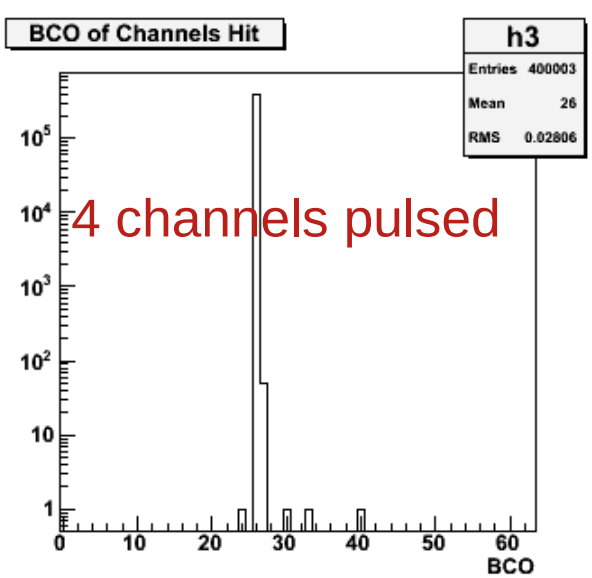


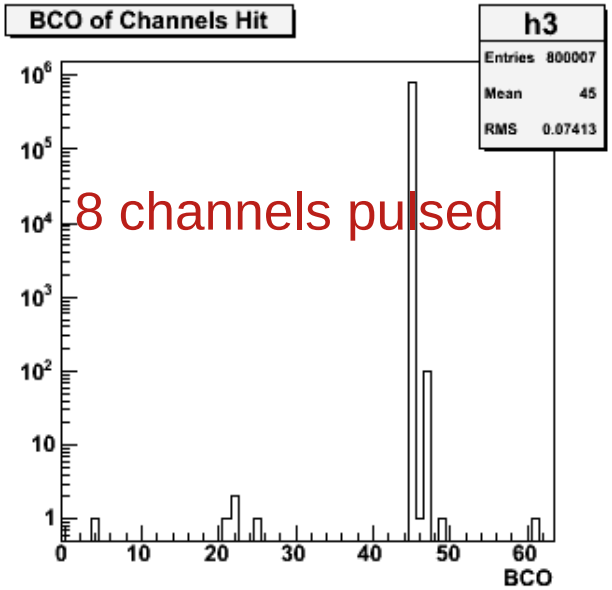
- Up to 4 hit strips can be read out in 4 beam clock cycles (4 x 106 ns)
- Hits are processed in a 4-phase architecture
- Access to the readout bus is controlled by token logic
- Data is pushed onto one or two LVDS serial outputs lines (user selected)
- Data output word is 20 bits
- Output word includes channel ID, 3-bits ADC, time stamp
- Sync word is provided to synchronize DAQ, 1 “sync bit” followed by 19 zeroes
- Serial data output clock is 200 MHz
- Channels can be masked off in any pattern (programmable)
- Output data is zero-suppressed
- FIFO is 20 bits wide and 32 words deep
- Slow control is a serial read/write interface to the FPHX, 32-bit word, clocked at 10 MHz

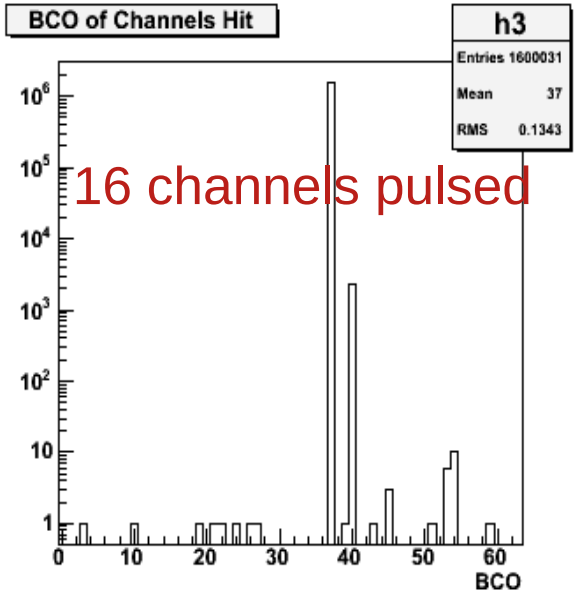
FPHX-1 Tests

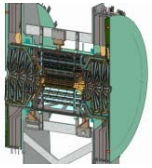


- **FPHX-1 "freeze-frame" issue caused multiple BCOs to be produced when >4 channels were pulsed at one time**
- **Jim Hoff (FPHX digital designer) was able to simulate and confirm that there was a bug in the logic**







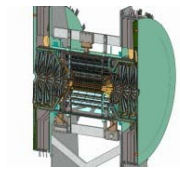


FPHX Changes for 2nd MOSIS Prototype submitted June 3, 2009 Delivered in August, 2009

- **Threshold dispersion reduction (shown at last review)**
- **Increase channel gain settings: 46,50,60,67,85,100,150,200,mV/fC**
- **W/L input transistor selection optimized**
- **Enable R/O on either serial output line, serialout1 or serialout2 or both**
- **Add 7th time stamp bit (drop last word bit - we don't use it)**
- **Fix the logic bug that Jim Hoff found that results in a mis-id of time-stamped events under certain timing conditions**

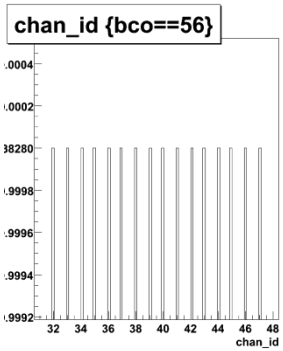
Updated FPHX2 Chip Documentation sent on June 4, 2009 and it is posted on the FVTX Twiki (FPHX2_June2009Revision.doc)

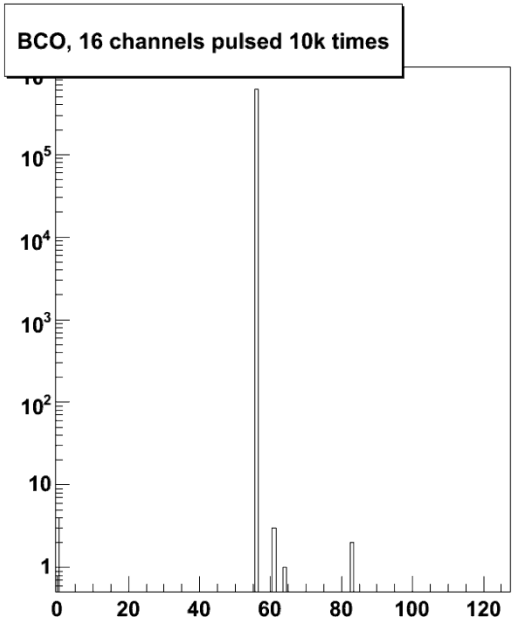
FPHX-2 Tests of Freeze-Frame

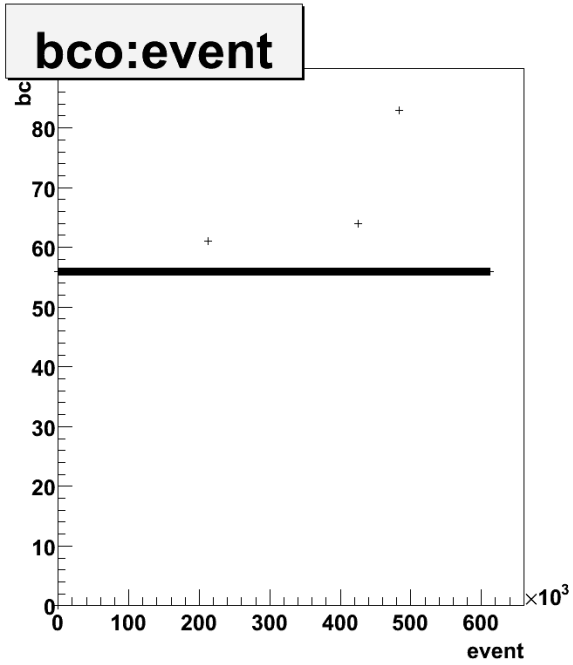


- **FPHX-2 does not have the freeze-frame issue :**
- **8 channels pulsed – only 2 events with non-pulser BCO, came at very end of event collection**
- **16 channels pulsed – just few odd events with non-pulser BCO. When selecting pulser-BCO, channel ID distribution has exactly same number of hits in each channel.**

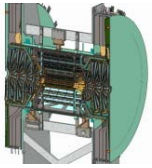
16 channels pulsed







FPHX2 Tests of Threshold Dispersion

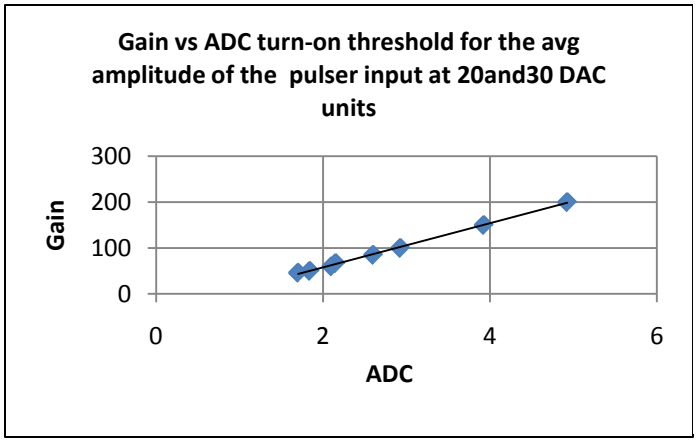


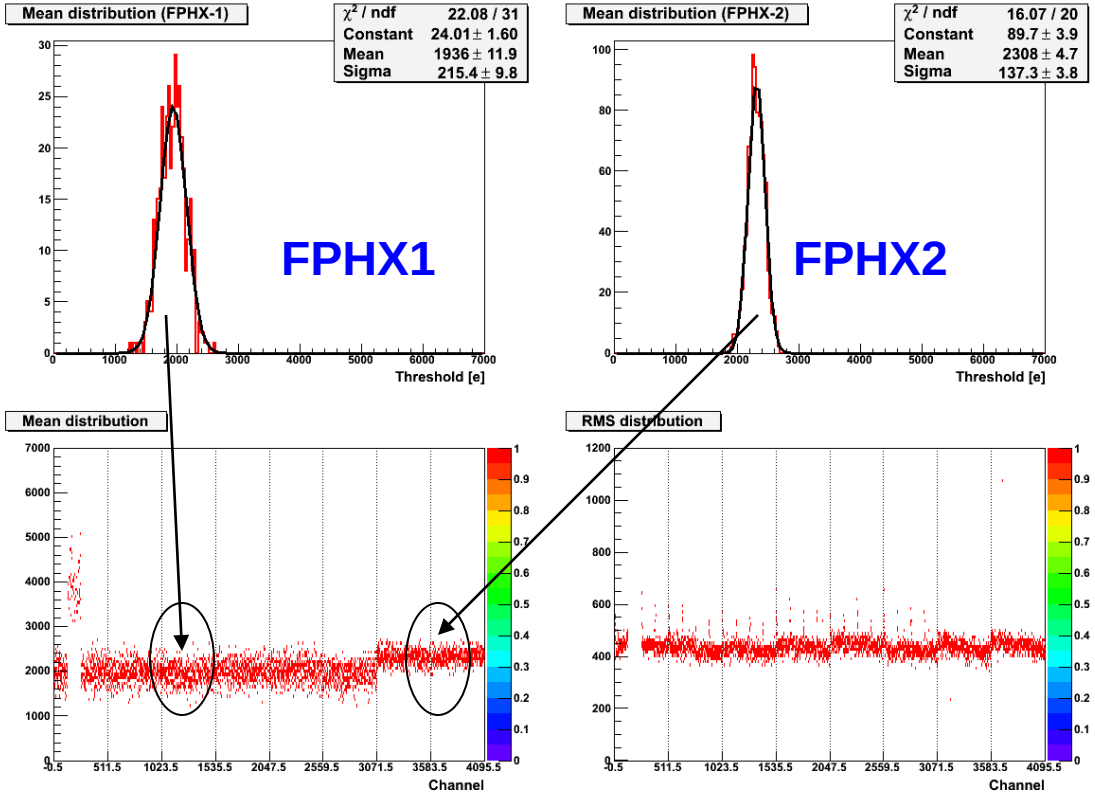
- **FPHX-1: GSel<1:0>:** determines integrator feedback capacitance Cfb = 25fF + [(25fF)(GSel)].
  Gain = 5*(1/Cfb)*100 in mV/fC→ Gsel=0:2→ Gain = 200, **100**, 65, 50 mV/fC

- **FPHX-2: GSel<2:0>:** determines integrator feedback capacitance Cfb = 25fF + [(8.6fF)(GSel<0>) + (25fF)(GSel<1>) + (50fF)(GSel<2>)].
  Gain = 5*(1/Cfb)*100 in mV/fC→ Gsel=0:7→ Gain = 200, 150, **100**, 85, 65, 60, 50, 46 mV/fC

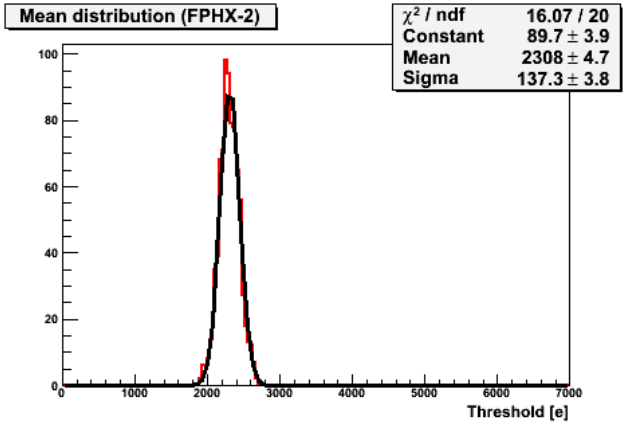
- **FPHX-1 with GSel = 1(100 mV/fC)**
  - **Threshold Mean = 1936 e**
  - **Threshold RMS = 215 e**
- **FPHX-2 with GSel = 2(100 mV/fC)**
  - **Threshold Mean = 2308 e**
  - **Threshold RMS = 137 e**

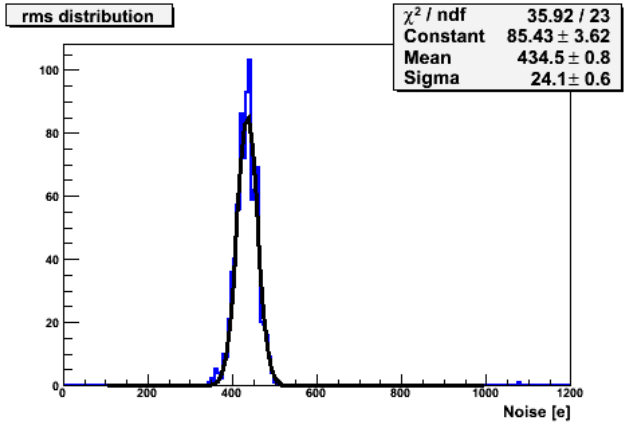
Threshold dispersion reduced by 40%

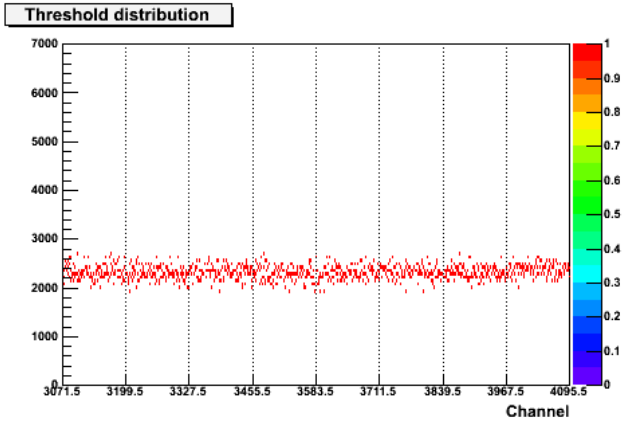


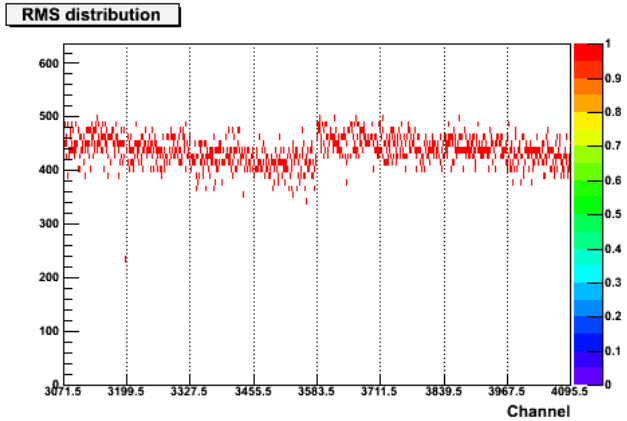


FPHX2 Noise Test







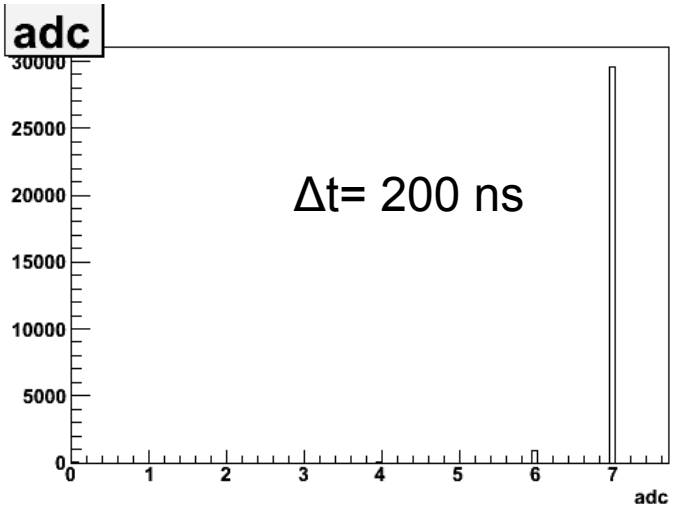


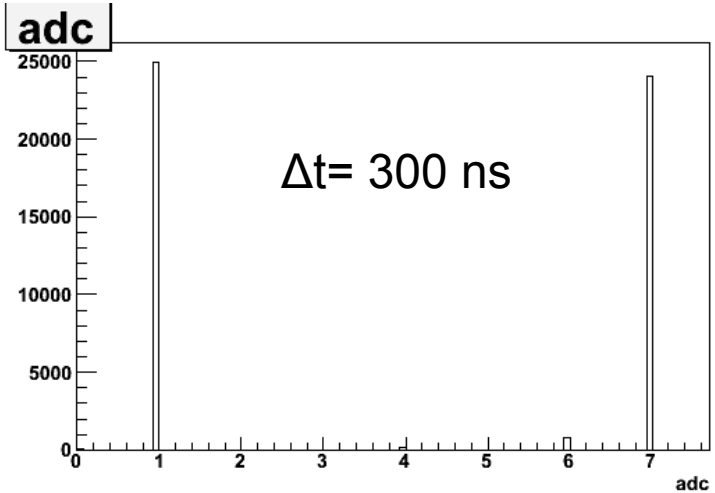
Noise mean 435 e's

(spec-115 e's +134/pf)

Noise rms 24 e's

Pulse pair response



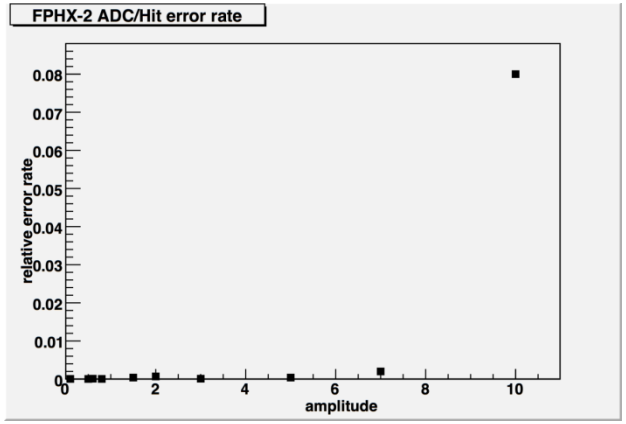


Pulse pair, 1500 and 150 mV

Fully efficient for 2nd hit at 300 ns

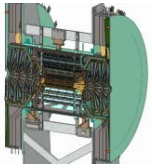
Overdrive response

- **Use Tek waveform gen. to deliver very large clean pulses**
- **Study relative rate of incorrect ADC values (mainly extra hits with low ADC values)**
- **Front end is robust and not easily damaged**



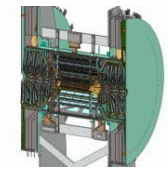
Negligible error rate below 5V or ~1E6 e^-

FPHX Test results summary

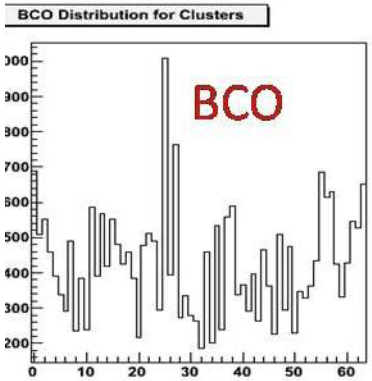


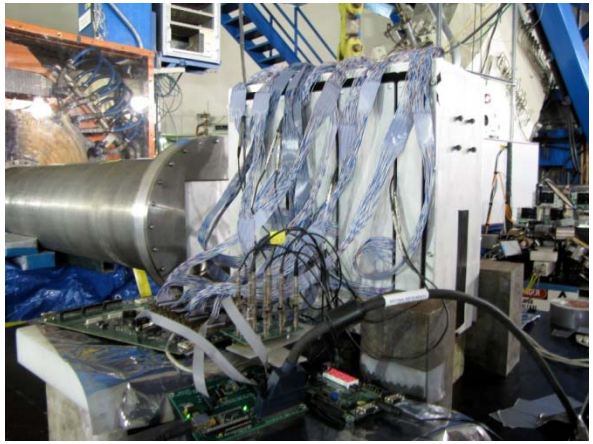
- Integrator and shaper responses are according to specifications
    - gain verified 46, 50, 60, 66, 85, 100, 150 or 200 mV/fC
    - dynamic range > 800 mV (non-linear from ~800mV to 1V)
    - nominal peaking time 60 ns
    - noise is acceptable ~115 e's + ~ 134 e's/pf
    - no measureable crosstalk to neighbor channels with large signal input
    - all programmable bits functions were verified
    - FPHX operates in a predictable and stable mode over a wide range of setup parameters
    - Power ~ 140 uW/ch analog plus ~ 300 µW/ch digital – acceptable
- Comparator response linear to ~ 1%
- Threshold dispersion ~137 e's rms
- Two pulse resolution ~300 ns
- Operates reliably with 10 MHz BCO and 200 MHz readout under a variety of conditions
- Conclusion
    - all relevant FPHX performance parameters have been measured and exercised sufficiently to give us confidence that the chip performs to specification
    - PHENIX review panel recommends to proceed to full production

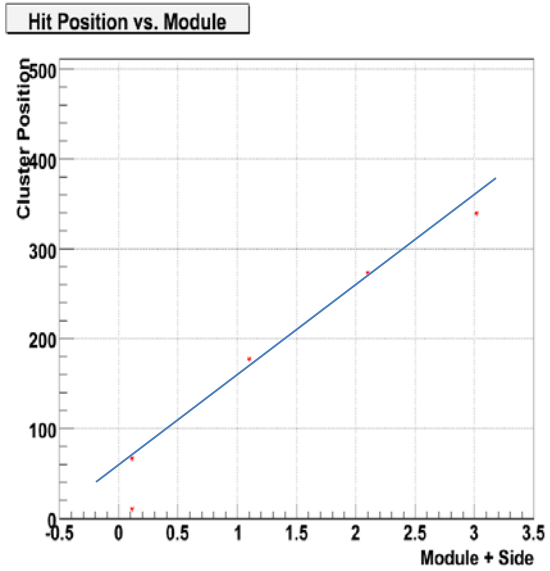
Beam test multiplicities were too high, but detectors and readout worked correctly

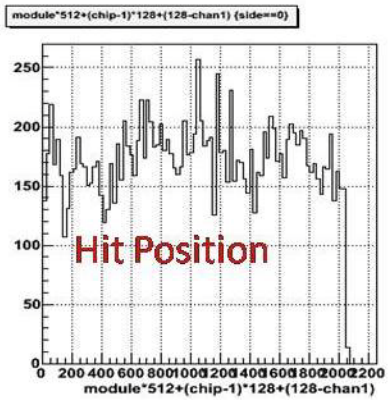


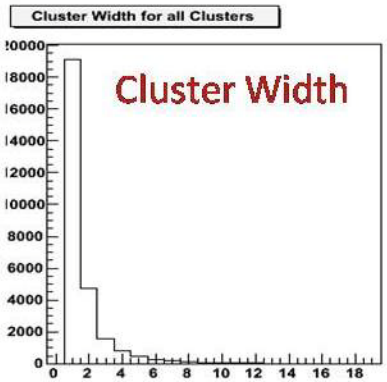
- BCO, hit distributions flat within statistics
- Reasonable number of 1,2,3 strip-wide clusters
- No readout hangups

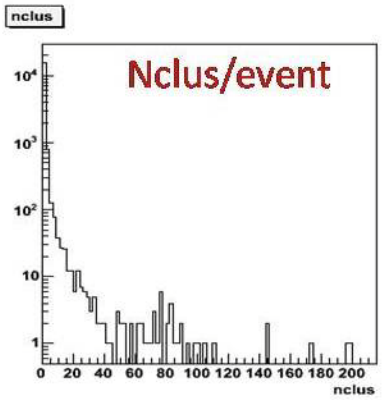




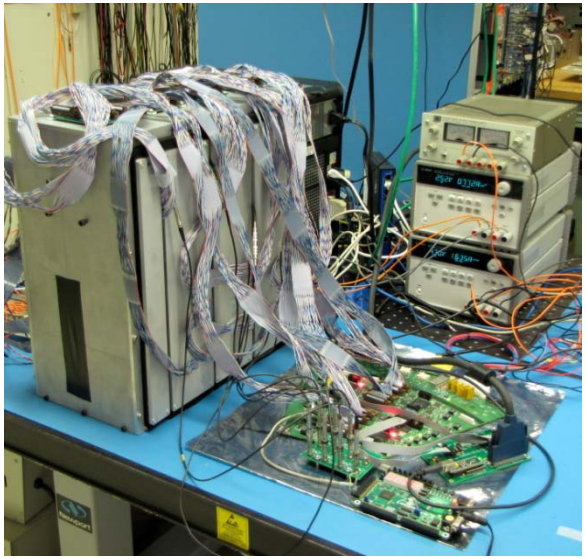


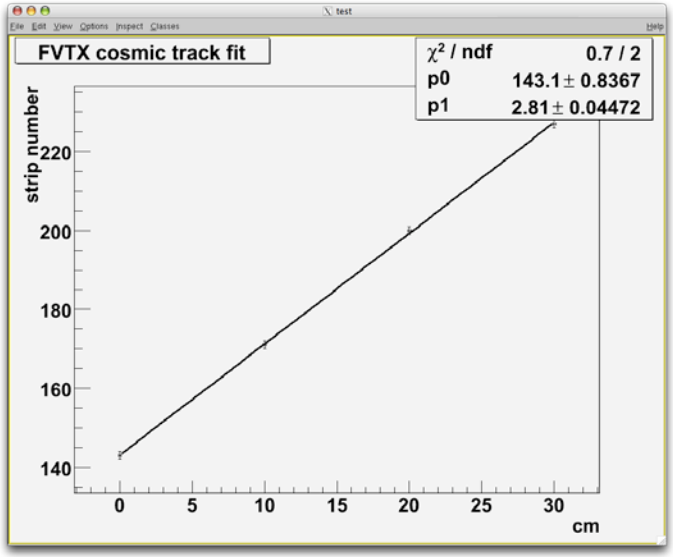


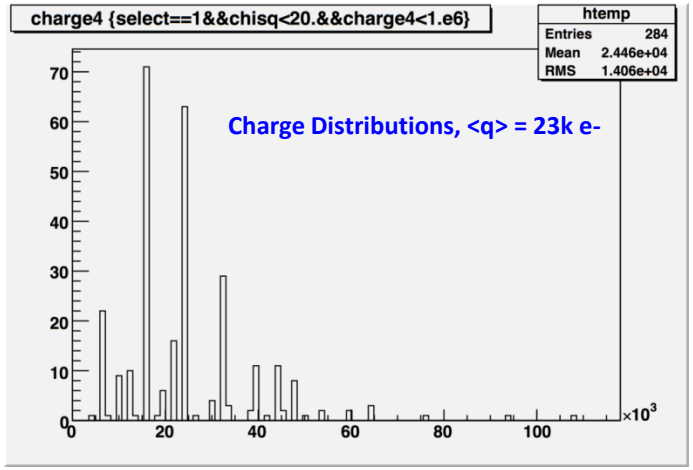


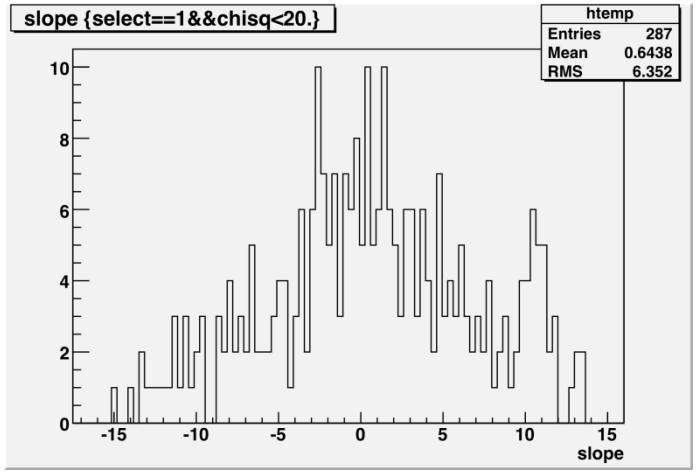


Track fit for cosmic rays



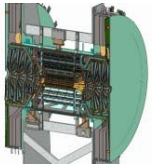






With position sigma of 1 strip in fit

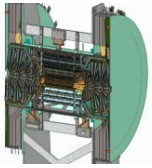
Good tracks are obviously straight with small χ^2



Beam and Cosmic Ray Wedge Tests Summary

- FPHX operates reliably even in harsh conditions
- Cluster charge, positions are as expected
- Resolutions extracted from tracks are sub-strip size
- Good efficiencies extracted (>97%)
- No issues with DAQ systems in beam or cosmic environment

Schedule For Sensors



Initial Prototype, ON-Semi – May, 2007

Current Prototype, Hamamatsu – shipped 31 October, 2008

Production Order submitted to Hamamatsu October, 2009

Production delivery 3-to-5 months ARO (partial deliveries)

Production order:

343 Large Wedge Sensors

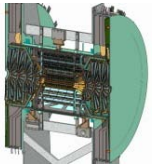
- 288 installed in FVTX
- 55 spares

120 Small Wedge Sensors

- 96 installed in FVTX
- 24 spares

WBS	Item	Date
1.4.1.2.1	Design prototype sensor mask	07/08/08 done
1.4.1.2.2	Process prototype sensors	10/28/08 done
1.4.1.2.3	Test prototypes	02/10/09 done
1.4.1.2.4	Wire-bond sensor to FPHX	04/10/09 done
1.4.1.3.1	Submit production sensors	10/23/09 done
1.4.1.3.2	QA production sensors	04/20/2010 Finish date

FPHX Schedule



Production order:

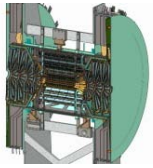
24 wafers (approx. 20,000 die)

8448 installed in FVTX

Wafer Probe tests at FNAL – Al Baumbaugh

- **FNAL designed FPHX-specific probe card (3 each on order)**
- **FNAL is developing control software to run the probe station**
- **FNAL is developing software to run test program on the probe station**
- **All registers will be written to and read back**
- **Pulser scan tests will be run for each die**
- **Bad chips will be inked**
- **All test results written to a database**

WBS	item	Date
1.4.2.3	FPHX layout design	04/10/08 done
1.4.2.6	Design review	04/14/08 done
1.4.2.4.1	Submission to MOSIS	08/22/08 done
1.4.2.4.2	Prototype tests	10/10/08 done
1.4.2.4.3, 1.4.2.4.4	Submit second prototype run	07/31/09 done
1.4.2.4.5	Test second prototype	09/25/09 done
1.4.2.4.9	Second run performance review	10/01/09 done
1.4.2.5.1	Submit engineering run (production run)	12/17/09 done
1.4.2.5.2	Test production wafers	02/04/10 Finish date



Summary

- Sensors prototyped and extensively tested – no issues uncovered
- FPHX prototyped in two rounds and extensively tested – performs to specifications
- Sensor + FPHX wedge operates as expected and has proved to be robust and reliable under a variety of conditions
- Sensors and FPHX chips have been submitted for production – a significant reduction in technical risk to the Project