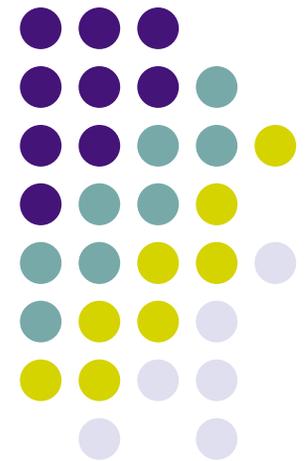


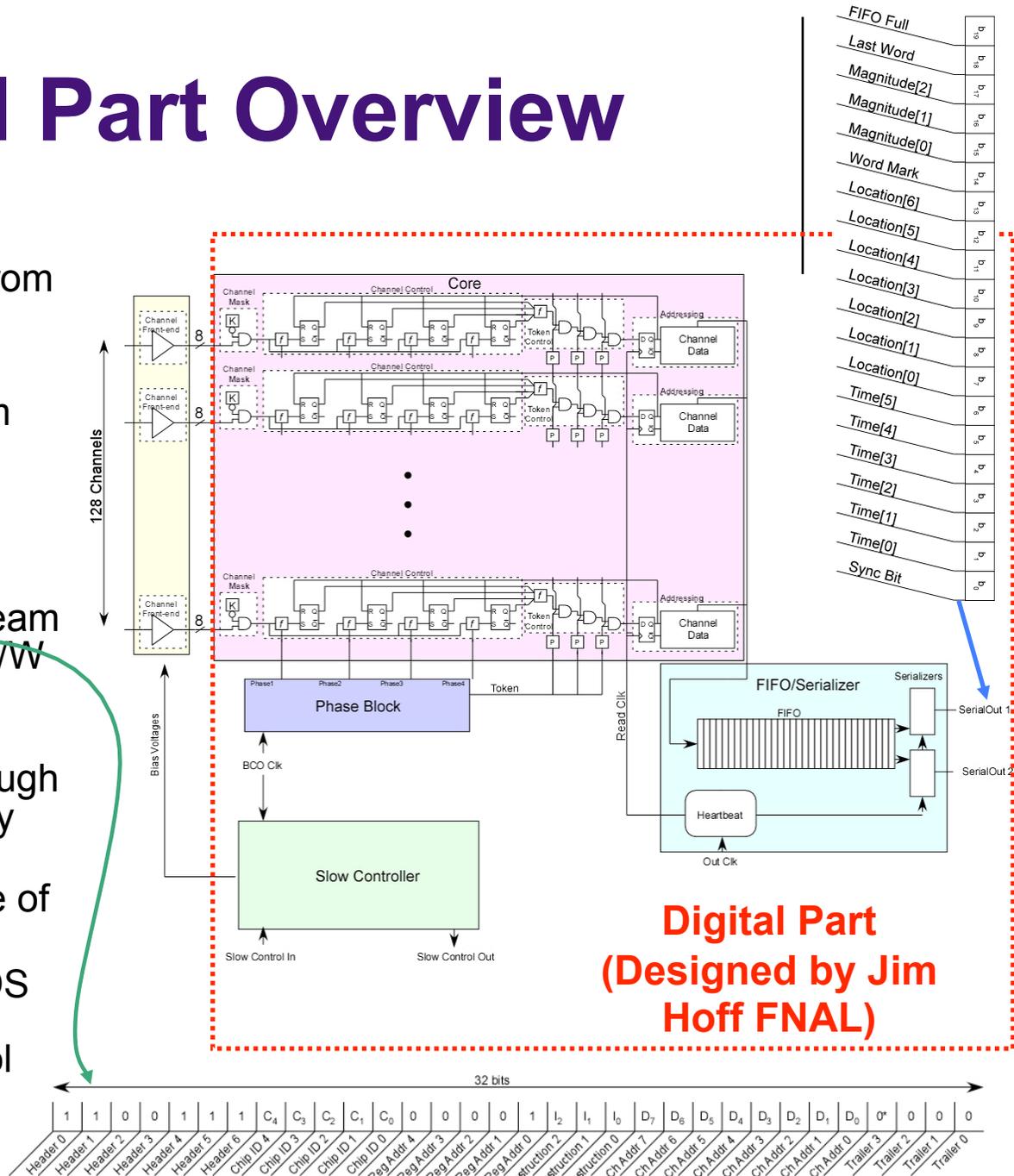
FPHX Digital Design Tests

LANL



FPHX Digital Part Overview

- Most important features
 - Completely independent from Front End
 - Data Push architecture
 - Core operates at 20xBeam Clock
 - Phase of main clock and beam clock important for Phase Block
 - Slow Controller runs by Beam Clock, 32 bit 1line serial R/W interface
 - FIFO ships the data out serially on main clock through either 2 output lines or only line 1
 - Data outputted at max rate of 4 hits/ BCO clock
 - Main core reset as an LVDS input + 3 separate smart resets through slow control



1	1	0	0	1	1	1	C ₄	C ₃	C ₂	C ₁	C ₀	0	0	0	0	0	0	1	I ₂	I ₁	I ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	0 [*]	0	0	0
Header 0	Header 1	Header 2	Header 3	Header 4	Header 5	Header 6	Chip ID 4	Chip ID 3	Chip ID 2	Chip ID 1	Chip ID 0	Reg Addr 4	Reg Addr 3	Reg Addr 2	Reg Addr 1	Reg Addr 0	Instruction 2	Instruction 1	Instruction 0	Ch Addr 7	Ch Addr 6	Ch Addr 5	Ch Addr 4	Ch Addr 3	Ch Addr 2	Ch Addr 1	Ch Addr 0	Trailer 3	Trailer 2	Trailer 1	Trailer 0		

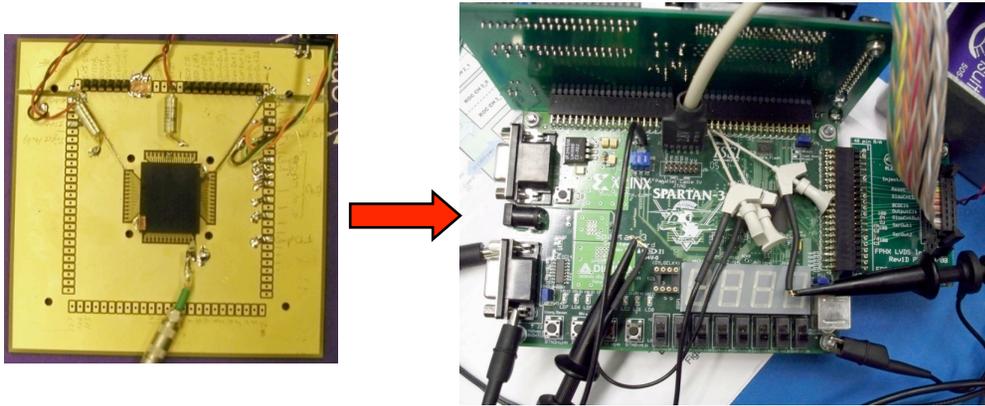
List of Tasks

Completion Status



- **The list below was proposed prior to chip delivery. Most of the tests finished**
- **Core and Output FIFO/Serializer**
 - Test readout at full speed **YES**
 - Clock operations: interference, noise, phasing sensitivity **YES**
 - Threshold scan **YES**
 - Mask pattern tests **YES**
 - Successive beam clock hit response **NO**
 - Power consumption under different setup configurations **YES**
 - Pointer operation **YES**
 - FIFO full response **YES**
 - Stability of the Beam Clock Counter **YES**
 - Phase sensitivity of the reset to clock **YES**
- **Slow Controller**
 - Read/write registers **YES**
 - Resets **YES**
 - Mask bits **YES**
 - Wild card function **YES**
 - Serial data output, one and two channel operation **YES**

Stating Point 09/28/08



- Received 1 FPHX Chip wire bonded to a custom made board on August 2008
- Over summer 2008 developed the test stand, consisting of: Xilinx Spartan-3 evaluation board, interface board, pulser board and NI DAQ board
- Once the chip arrived, the test setup was ready to operate the chip and read out the data



Test Stand Features



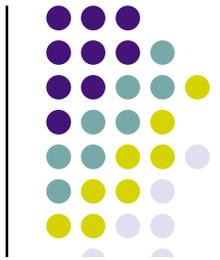
- Test stand is based on Xilinx Spartan3 FPGA
 - Coding – VHDL
 - RPM (Relative Placed Macros) blocks generated for fast design components, generated to operate at least at 210 MHz
 - 200 MHz and 10 MHz clocks generated by PLL from 50 MHz on-board oscillator
 - 2.5V LVDS signals used for communication
 - Pulser board generates predefined shape pulse of controllable amplitude. 3 control lines + trigger
 - 20 dB attenuator is used to lower noise on the analog pulser input
 - NI board reads 32 bit at 20 MHz clock
 - USB communication based on a packet similar to Arcnet protocol
 - Variable length data packets can be sent to a chip with a single bite readback

Calibration Chain

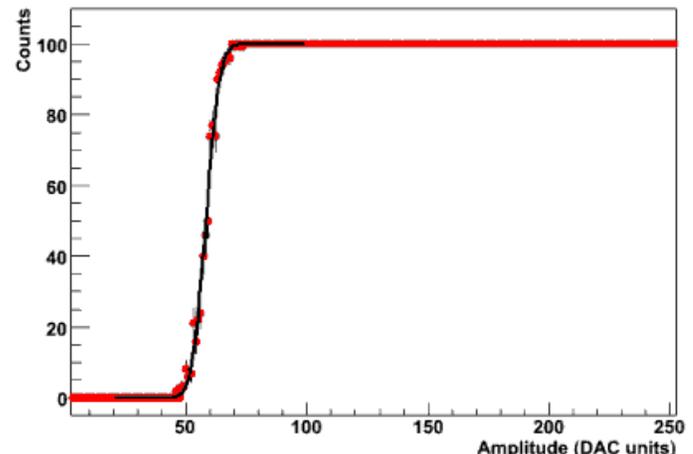
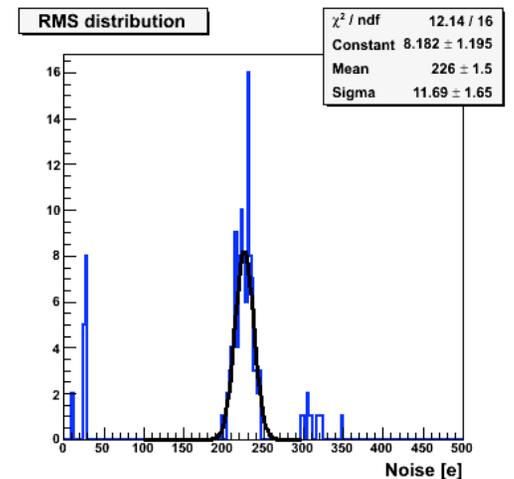
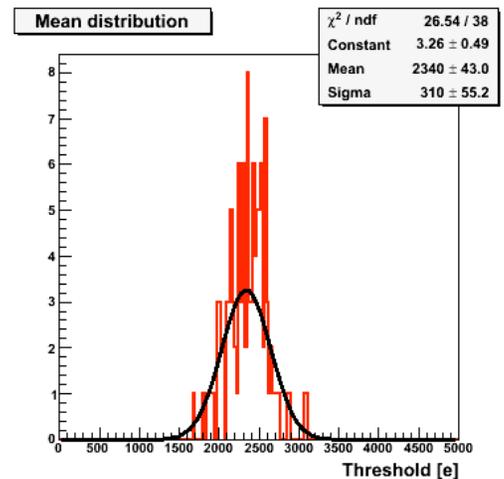


- During calibration chain the following sequence of events is generated inside the FPGA code:
 - Channel 0 is being unmasked (all the rest masked)
 - Amplitude is set to 0
 - 100 pulses sent with the current amplitude
 - Amplitude increments
 - If amplitude reaches maximum → Channel increments
 - If channel = 127 → everything stops
- At the same time read the data out:
 - If output buffer almost full – Issue BUSY which veto pulse generation
 - BUSY clears once Output buffer is empty
- Pulses sent with a spacing which maintains 64 clock periodicity

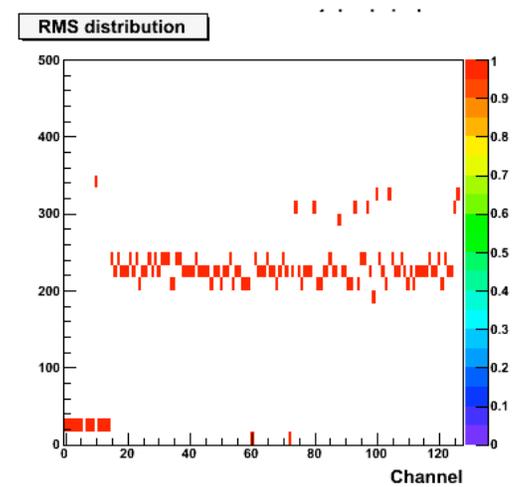
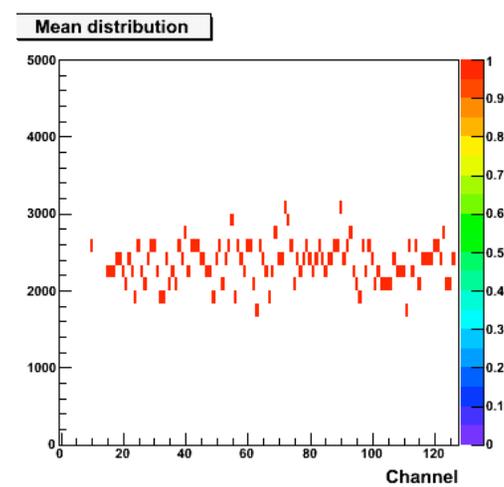
Calibration Results



- ~200 electrons noise on most channels
- Threshold turn-on and distribution width as expected
- Programmable comparator thresholds work
- Known issues with 1st 15 channels because comparators are bonded out
- Overall performance is consistent with design specifications



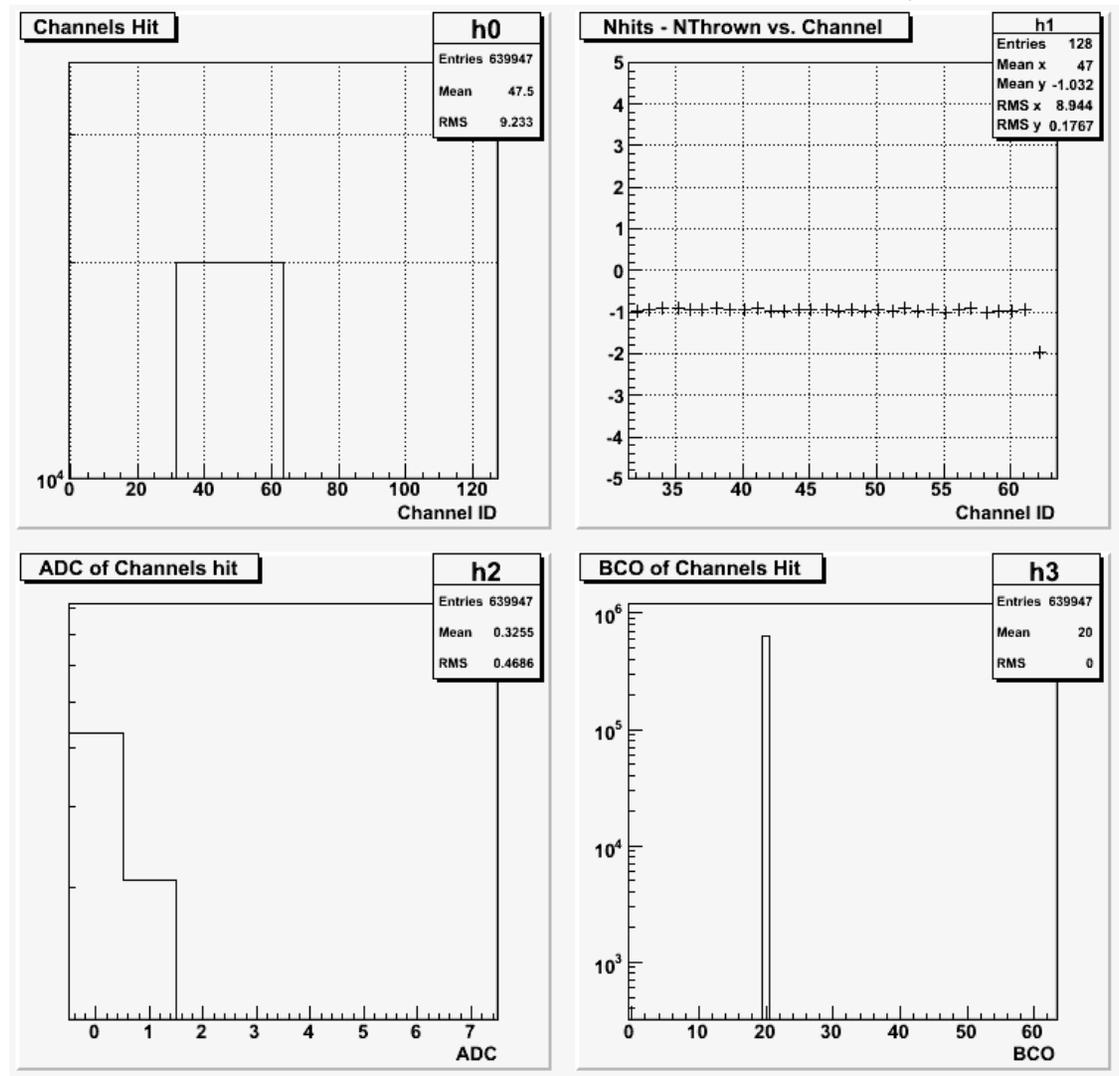
threshold turn-on curve



Hit Output Stability



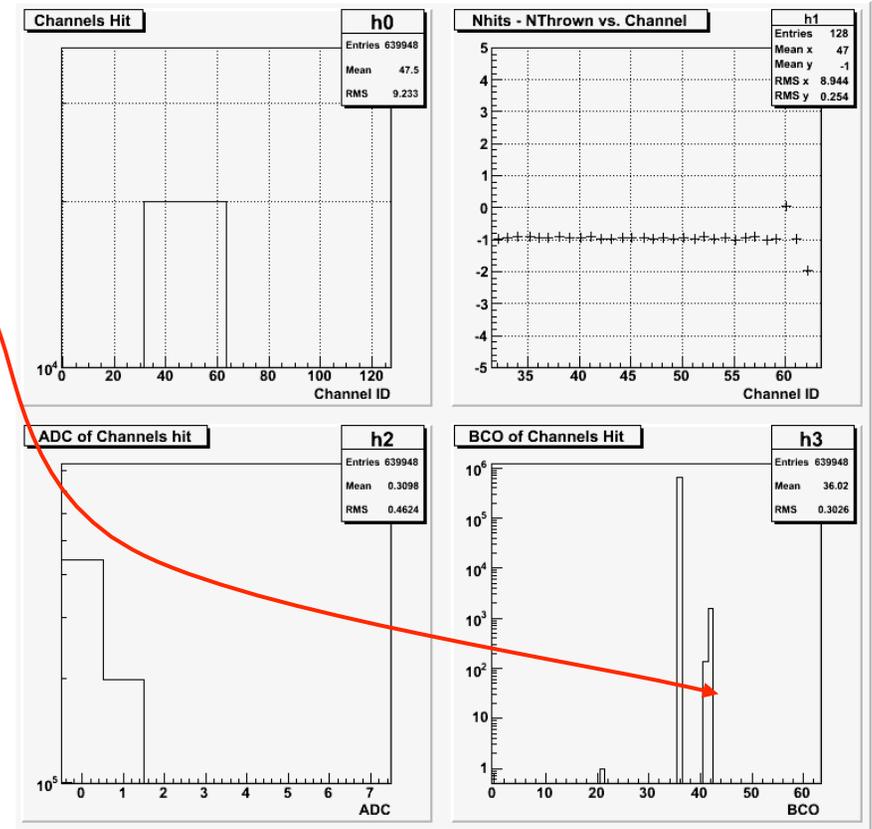
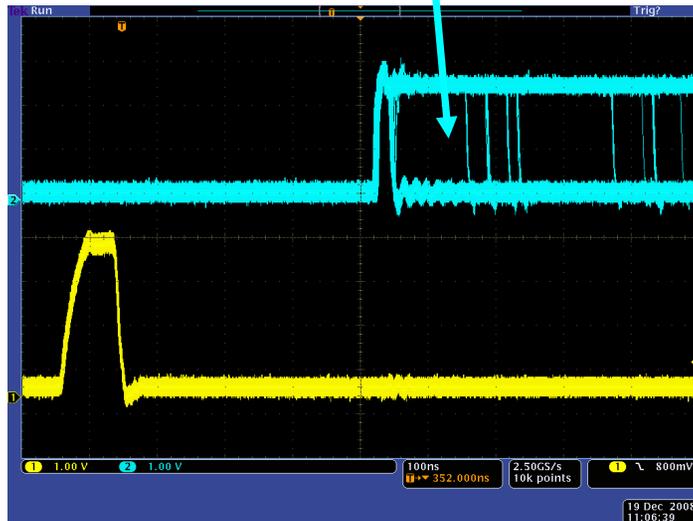
- A large number of pulses were generated with a particular BCO and sent into a number of channels
- BCO read from the data is constant (as it should be) and all the channels are equally populated
- Small discrepancy in one channel – readout software defect



Timing Studies



- The phase of the pulse wrt the edge of the clock was adjusted
- The problem was uncovered when the pulse was issued too close to the edge of the beam clock
- BCO assignment for the hits that leaks into the neighboring bucket is incorrect
- Also the GOTHIT signal becomes abnormally wide in this case





Register Read/Write

- Registers on the chip experienced a large number of read/write cycles during initialization and calibration
- So far no problems uncovered
- May be more rigorous tests are needed but would wait for more chips available for testing

Problems Found



- Only problem found is the storage of the BCO when pulses occur near a clock edge

Summary



- The list below was proposed prior to chip delivery. Most of the tests finished
- **Core and Output FIFO/Serializer**
 - Test readout at full speed **YES - true in all tests shown**
 - Clock operations: interference, noise, phasing sensitivity **YES - varied pulse->clock edge in tests**
 - Threshold scan **YES – 200 electron threshold variation. Tom Zimmerman will improve.**
 - Mask pattern tests **YES – series of channel masking exercised in all calibration tests**
 - Successive beam clock hit response **NO – cannot do with external pulser, need different approach**
 - Power consumption under different setup configurations **YES – consumption changed as expected**
 - Pointer operation **YES**
 - FIFO full response **YES – FIFO full bit comes out as it should with large events**
 - Stability of the Beam Clock Counter **YES – BCO stable with long train of pulses sent, different mask sets used. Only caveat: when pulse next to clock edge, does not work properly.**
 - Phase sensitivity of the reset to clock **YES – verified chip will not reset if sent on wrong clock edge**
- **Slow Controller**
 - Read/write registers **YES – exercised extensively in many weeks/months of testing**
 - Resets **YES**
 - Mask bits **YES – exercised extensively with calibration runs and other pulser runs**
 - Wild card function **YES – chip responds to wild-card address**
 - Serial data output, one and two channel operation **YES – data output responds to one/two channel operation. Only “surprise”: non-selected data line is not “quiet”; cannot choose which data line (0 or 1) outputs data in one channel operation.**