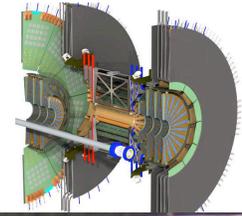


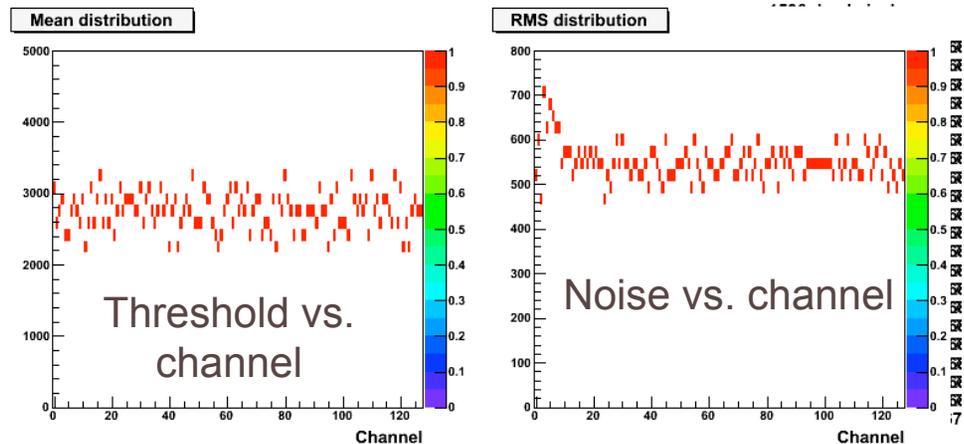
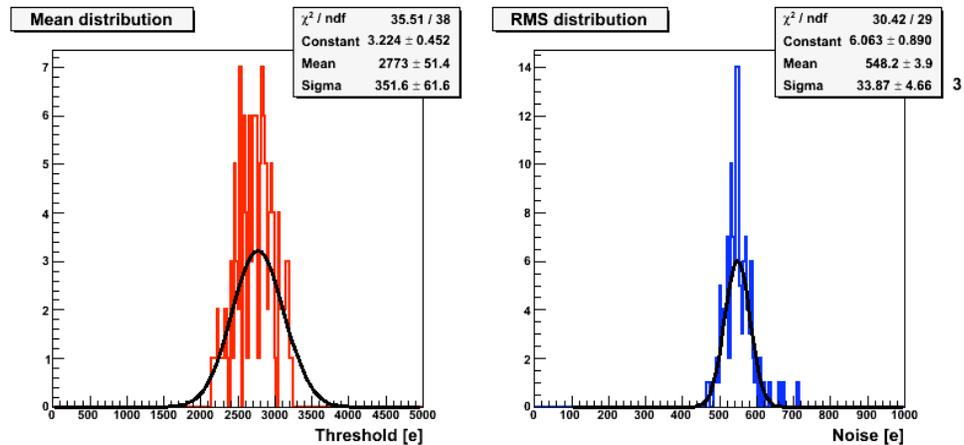
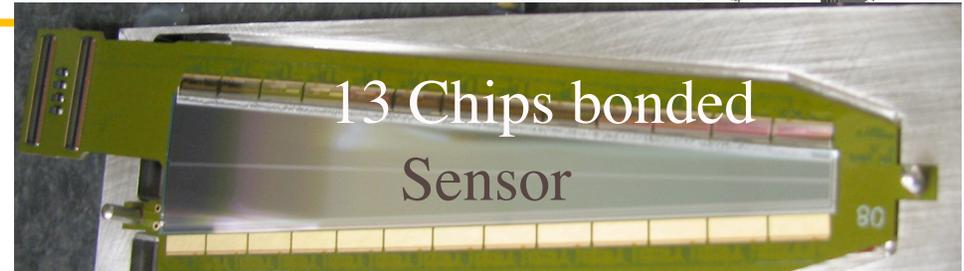
FVTX Monthly/Quarterly Report June, 2009

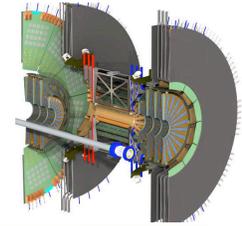
Technical Status, Cost & Schedule
Melynda Brooks, LANL



FPHX Wedge Tests

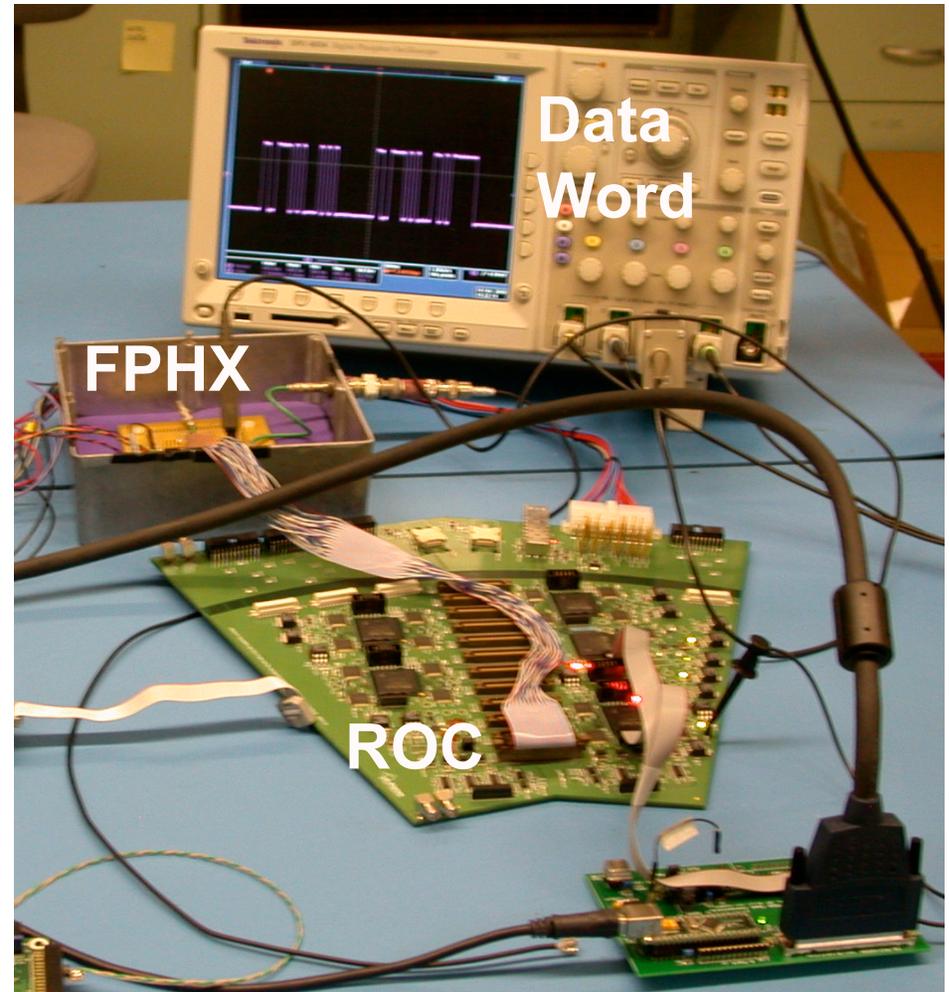
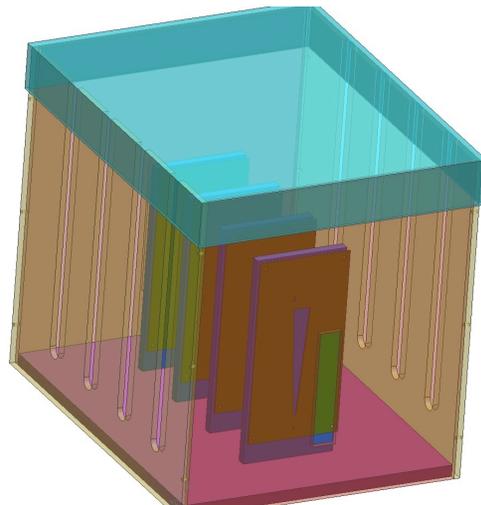
- 13-chip wedge tests revealed no new issues with FPHX design. Saw response to alpha, beta sources.
- Redesign work by FNAL on digital and analog changes (only one “bug” fix) **completed and new round submitted to MOSIS June 5, 2009**
- **Expect new FPHX chip available by end of July, beginning August**
- **In the mean time, we are preparing for beam test at LANL with multiple modules**
- **2 modules with 8 chips (4 each side), 1 PCB module with 17 chips (13+4), 1 kapton module with 15 chips) being assembled**





DAQ Status

- ROC continuing to be exercised through wedge tests
- Producing code to allow one ROC to read out 4 wedges in a test beam
- Clock distribution prototype board completed and delivered (distributes BCO to various ROC boards)
- Slow Controls interface board in progress
- FEM prototype expected ~end of July
- ROC 2nd round expected ~end of August

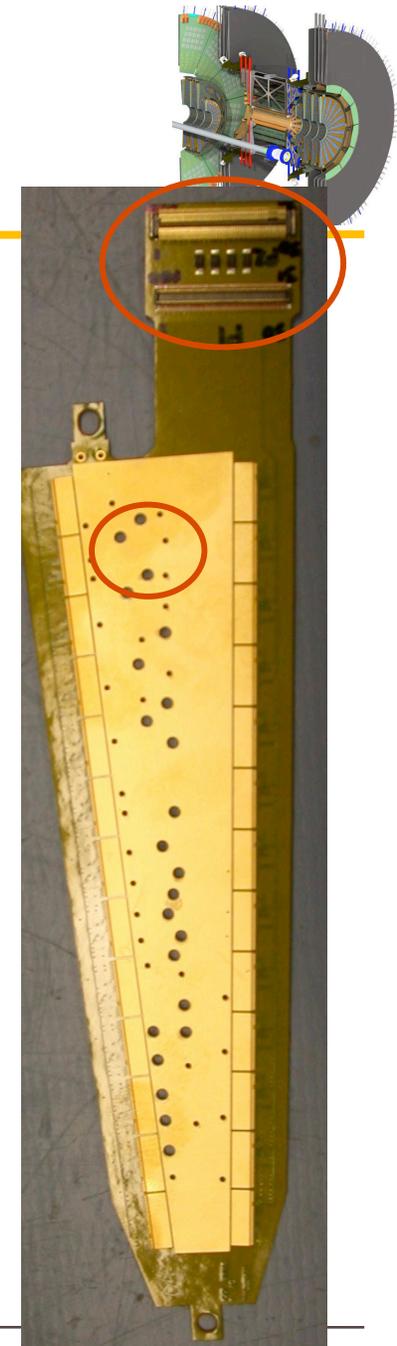


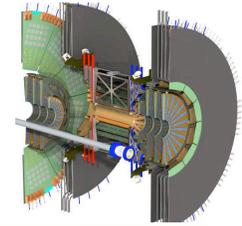
HDI Status

- Kapton HDI readout of 1 chip worked fine, even with pulsing to, activity from, all 13 chips
- Have read out 1 data line from 9 chips (1,2,3,4,5,7,9,11,13) and found no issues
- Now have interconnect board available which can read out all 13 chips.
- Sensor + 13 chips added to new kapton HDI which appears to have no sensor biasing issues. Will be tested after shipped from SiDet to UNM

SUMMARY:

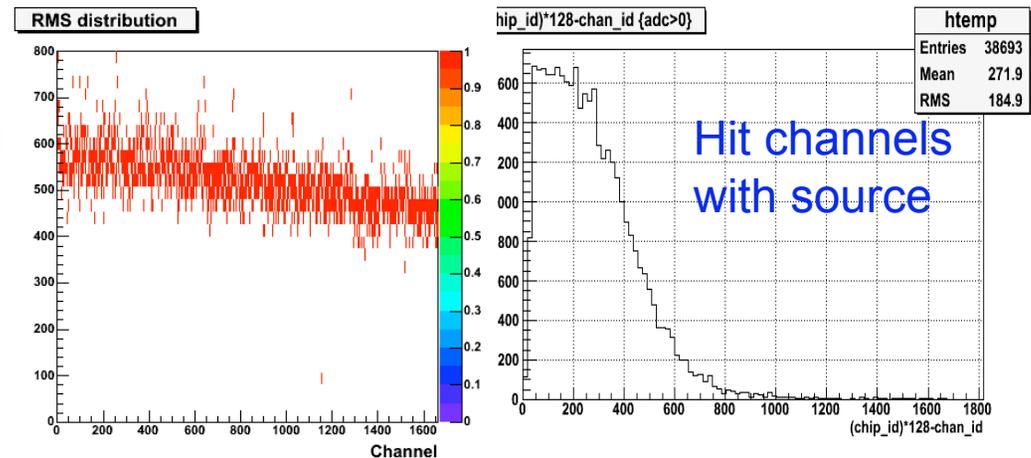
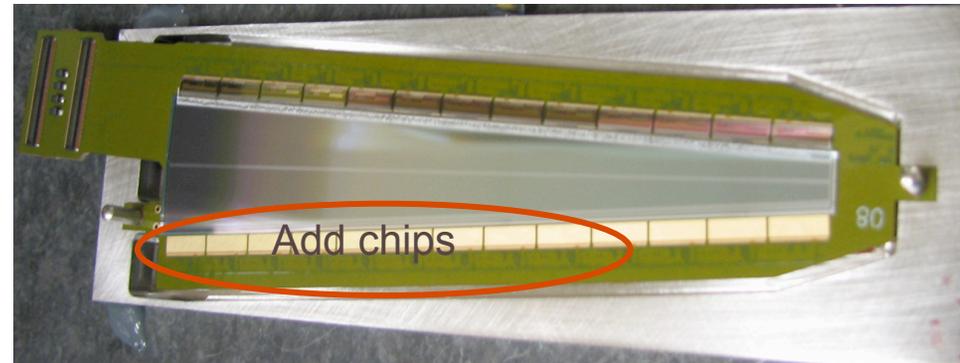
- no significant HDI design issues uncovered to date, but more kapton testing needed with sensor and 13 chips
- Some redesign work expected already though:
 - incorporate holes in middle of kapton electrical design,
 - some suggestions from Dyconex to improve manufacturability
 - May use single high-density connector instead of two

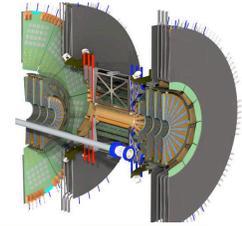




Sensor status

- Sensor fully tested in stand-alone tests previously.
- Sensor responds as expected in wedge tests (noise, source tests)
- Only test remaining is to look at response when chips are bonded to both sides of the sensor,
- Preparing for PR submission:
 - LANL procurement has checked PR and considers it in order
 - Final drawings of small sensor (not produced before) are being finalized
 - Hamamatsu will then be requested to re-quote
 - Expect process completed by ~end of June





Mechanical Status

Backplanes

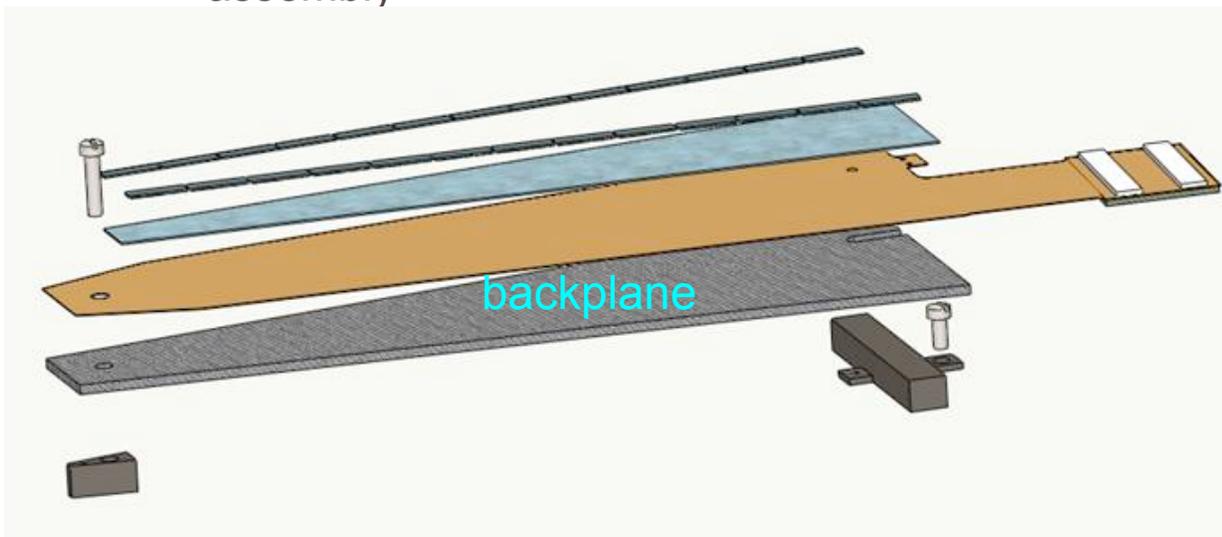
- Backplane procurement milestone: start procurement June 2009
- Received quote from LBNL (larger than previous quote), submitting SOW and will procure through BNL
- Final drawings in review

Cage and disks

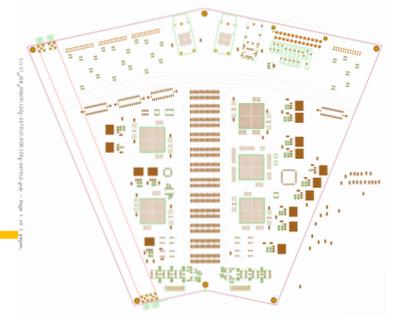
- Need to start procurement process also. Need new quote based on current drawings

Fixtures

- Some modifications to fixtures identified, to be implemented before production assembly



Production Procurements



Sensor order PR reopened at LANL:

- Everything is in order according to the purchasing department.
- Communicating with Hamamatsu for rebid.
- Expect order to be able to be placed when we want it placed

Backplanes:

- Final drawings available, (re)quote received from LBNL
- SOW submitted to BNL and PR submitted from their end

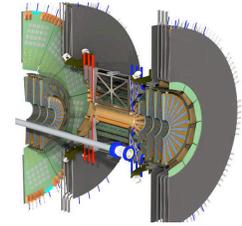
Wedge assembly:

- Draft quote and SOW from SiDet received
- Awaiting final quote from their budget department, but looks like assembly will fit into our MP budget

Disk/endcap assembly:

- Steve Pate identified testing equipment, clean room equipment, survey equipment required for assembly
- Many pieces of equipment on order or identified at BNL and being used to equip 2 assembly rooms

Cost & Schedule – mostly same info as May



Costs have been added since MP for:

- PCB HDI design and procurement
- Additional mechanical design work (\$30k)

Costs have been updated since MP for:

- HDI procurement
- Backplane and cage procurement – a new quote is +60k more than previous
- DAQ boards (refined estimates, but no manufacturer quote)
- Integration

Overall contingency = \$909k compared to \$927k from MP

Schedule – 2 months (of 5) lost on critical with June FPHX submission, but some may be gained back because MOSIS delivering chips faster now; still may investigate earlier engineering run than initially planned.